
Compact Models for Conductive and Convective Heat Transfer in Microelectronic Applications for the New Millenium

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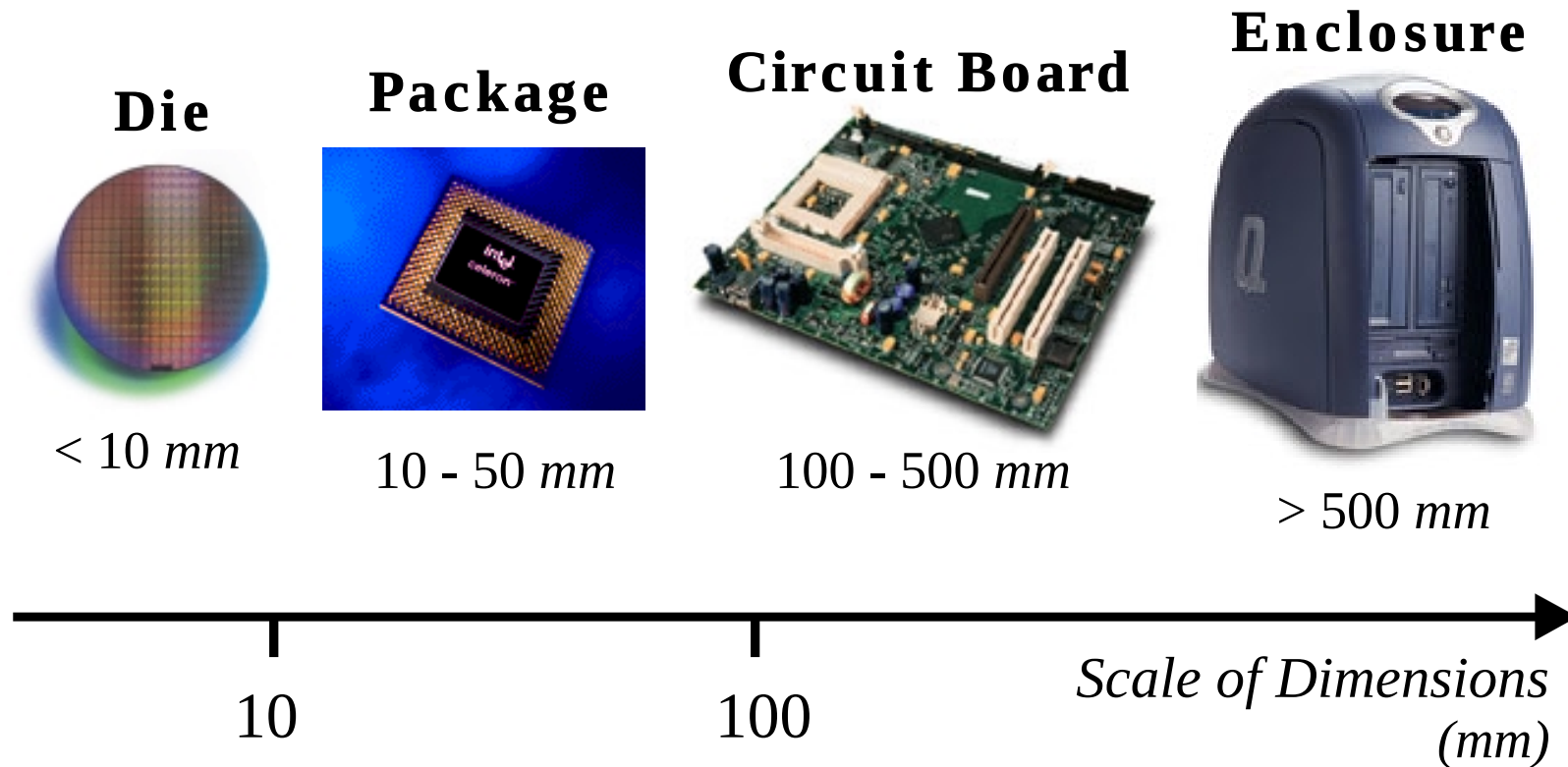


Outline

- Introduction
 - need for compact models
 - various types of compact models
- Examples of Compact Models
 - total resistance of multilayered substrates (vias)
 - natural convection in vented enclosures
 - natural convection plate fin heat sink
 - compact heat exchangers
- Concluding Remarks
- Future Directions



Microelectronic System Levels

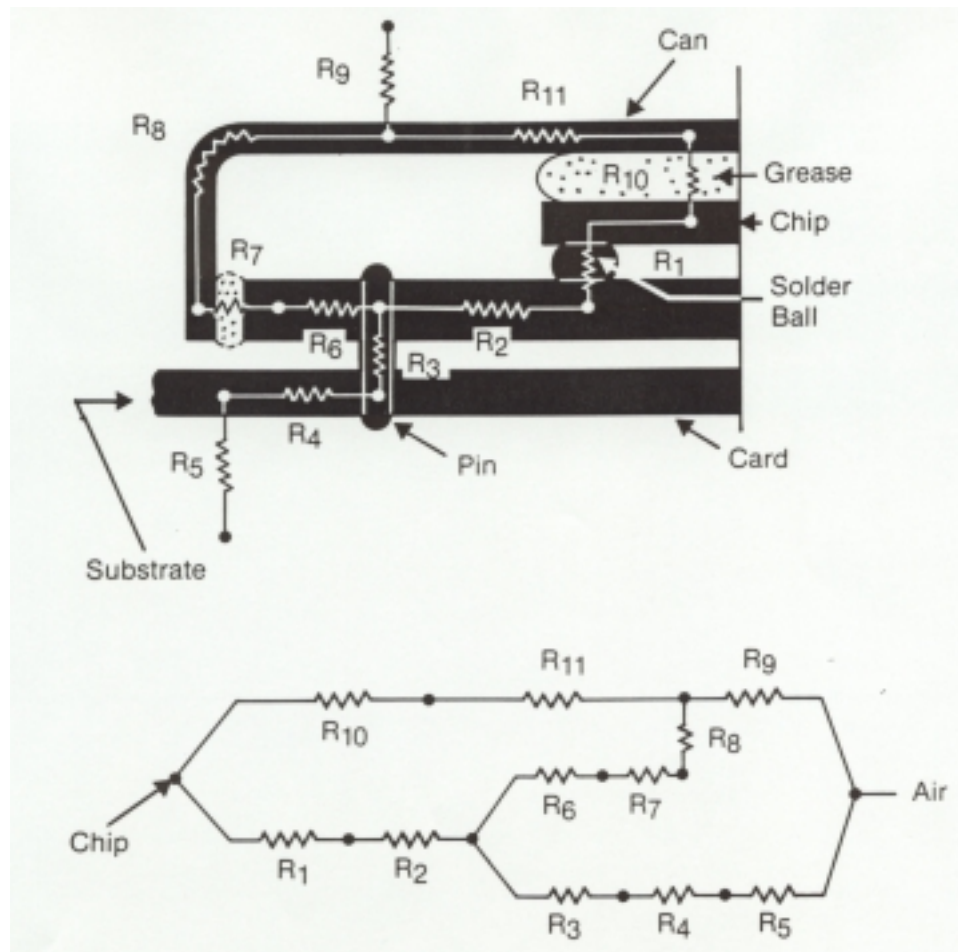


Compact Modeling Approaches

- Scale analysis
- Non-dimensionalization
- Thermal resistance modeling
- Combining asymptotic analytical solutions
- Development of bounds



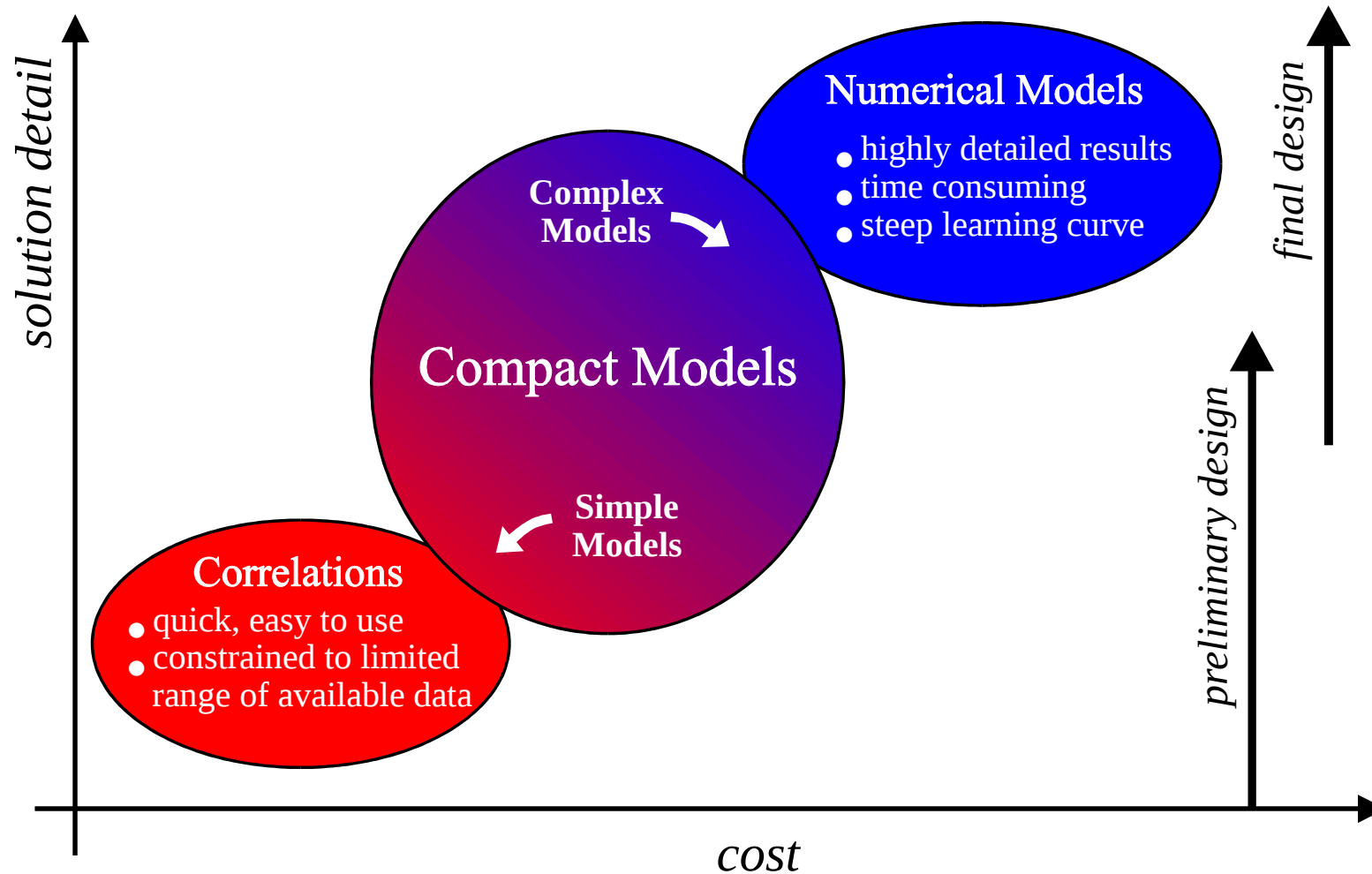
Thermal Resistance Modeling Example



R. C. Chu and R. E. Simons,
Thermal Management Concepts
in Microelectronic Packaging,
1984, pp. 193 - 214.



Introduction



Why Not Always Use Detailed Models?

- Detailed models have value because....
 - predict local temperature distribution within packages
 - allow designers to easily make parametric changes in model
 - DELPHI has proposed that they be the starting point for the creation of compact models
- However, detailed models also...
 - reveal internal (often proprietary) construction details of packages
 - are computationally demanding due to large grid required

S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.



Compact Models

- Compact models seek to capture the thermal behavior of the package accurately
 - at pre-determined critical points (junction, case etc.)
 - by using a reduced set of parameters to represent the package
- These parameters need not have a one-to-one correspondence with the package physical structure

S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.



What is (was) DELPHI?

- Project that proposed new methodologies for developing component computational models
- Ultimate Goal: to enable manufacturers to supply validated compact thermal models to end-users
- Results were:
 - detailed model understanding of several package types
 - 2 experimental systems (Double Cold Plate and Submerged Double Jet Impingement) for validation
 - compact model networks for several package types
 - a methodology to tie these together

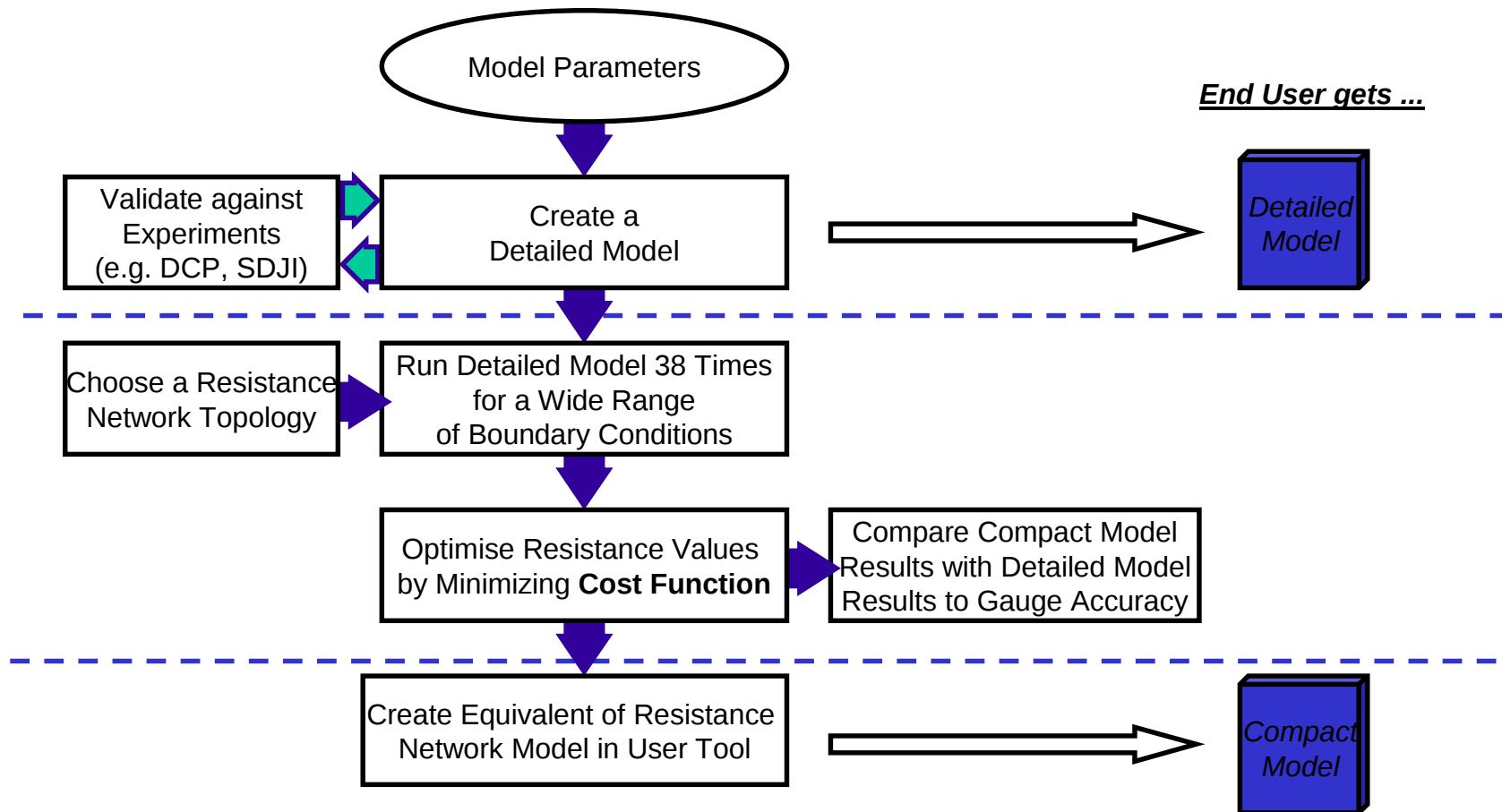
S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.



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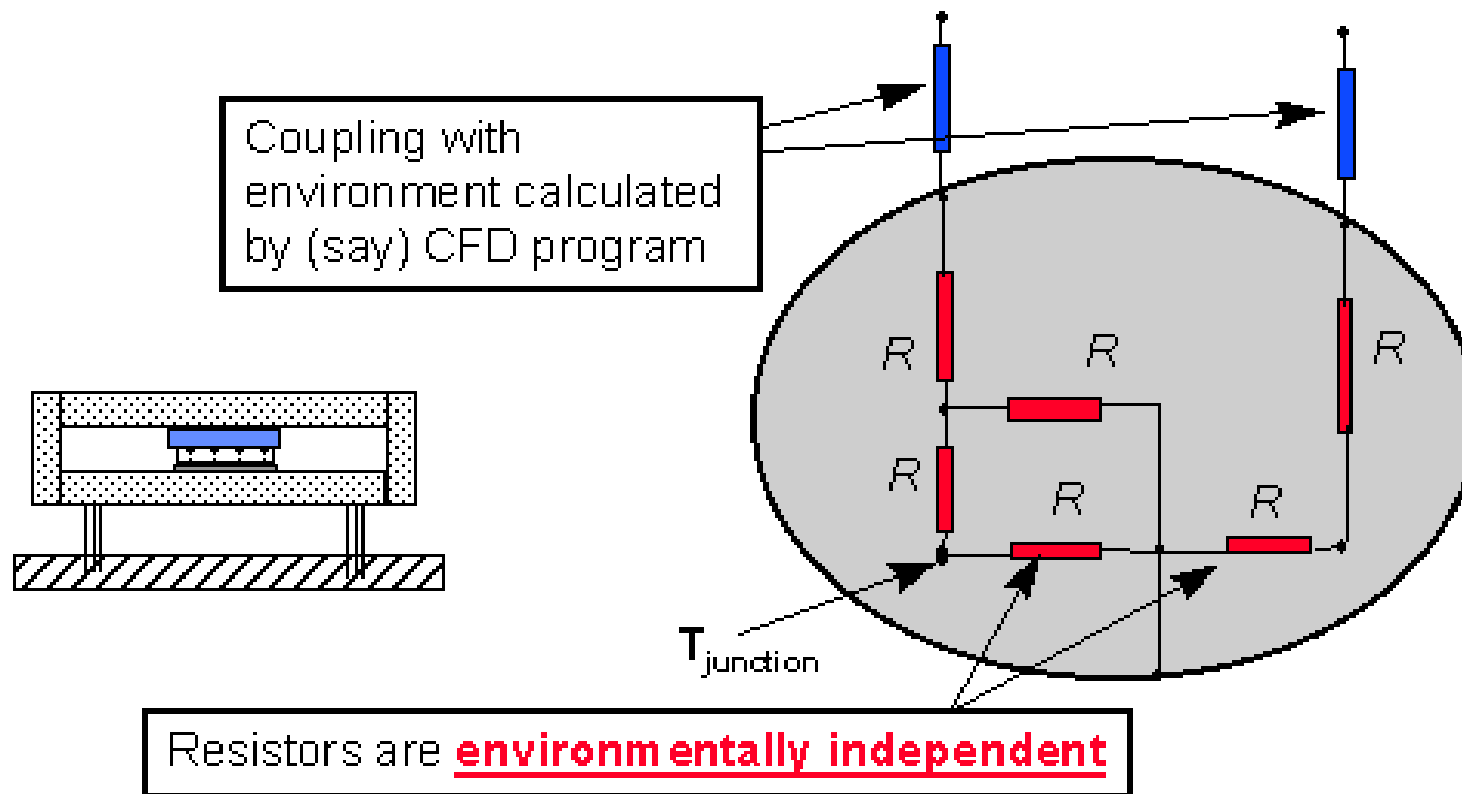
The DELPHI Methodology



S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.

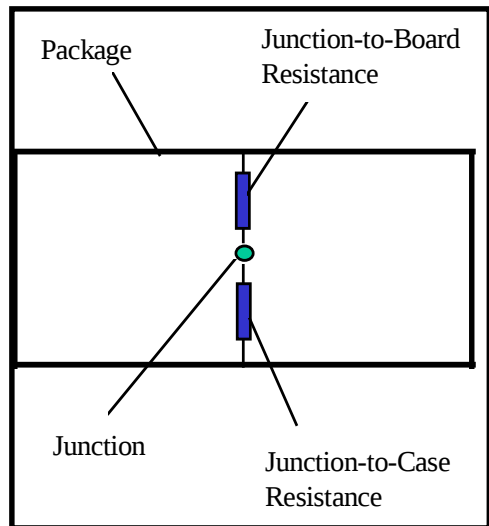


Boundary Condition Independent Resistance Networks

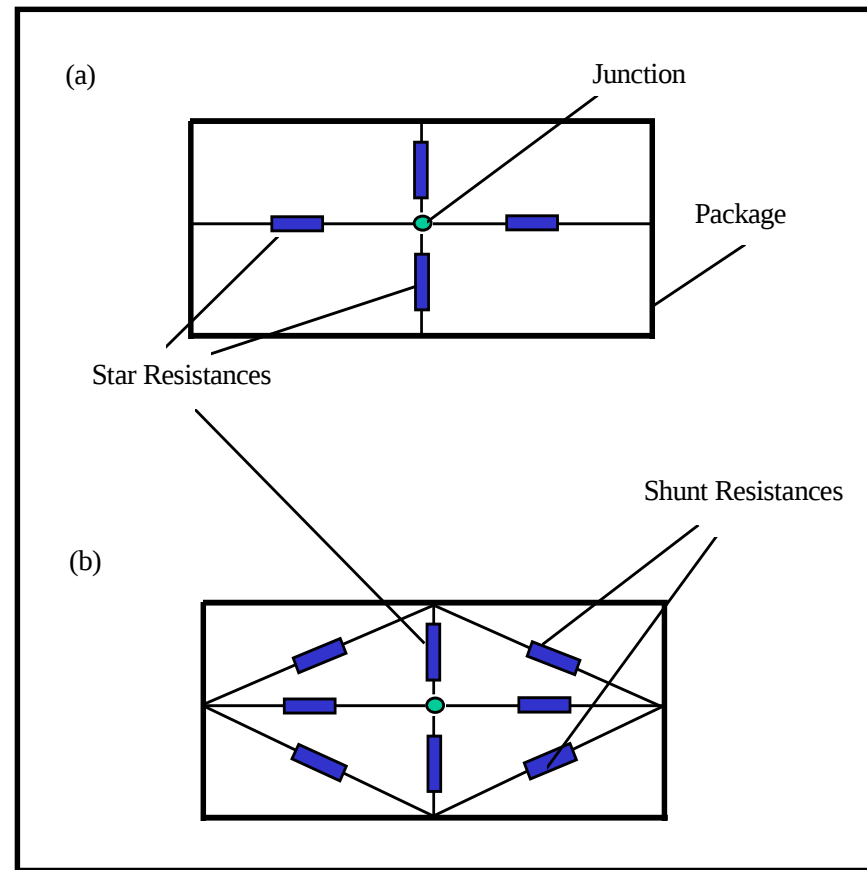


S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.

Network Topologies



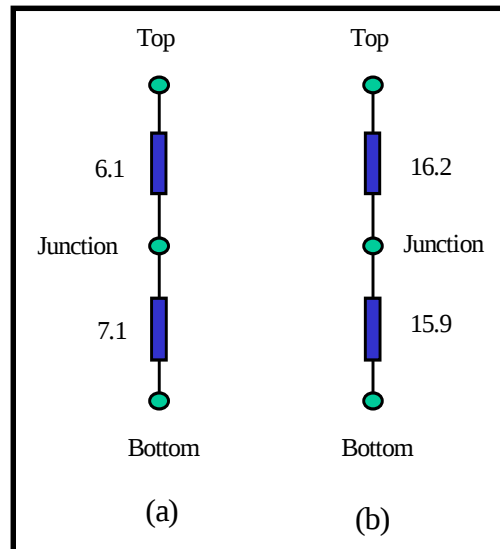
Two-Resistor



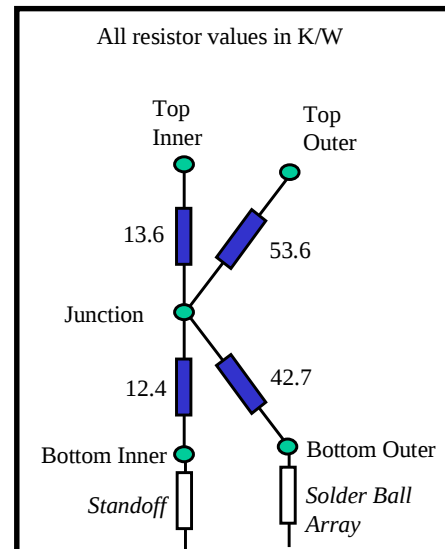
a) Star b) Shunt

S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.

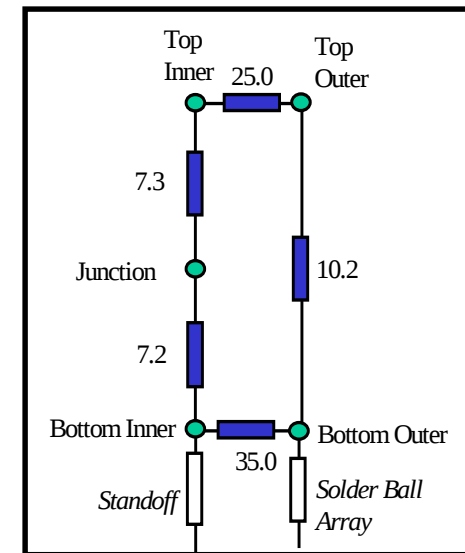
The Compact Models



Two Resistor Models
a) 2-Point Cold Plate Test
b) DELPHI Optimized

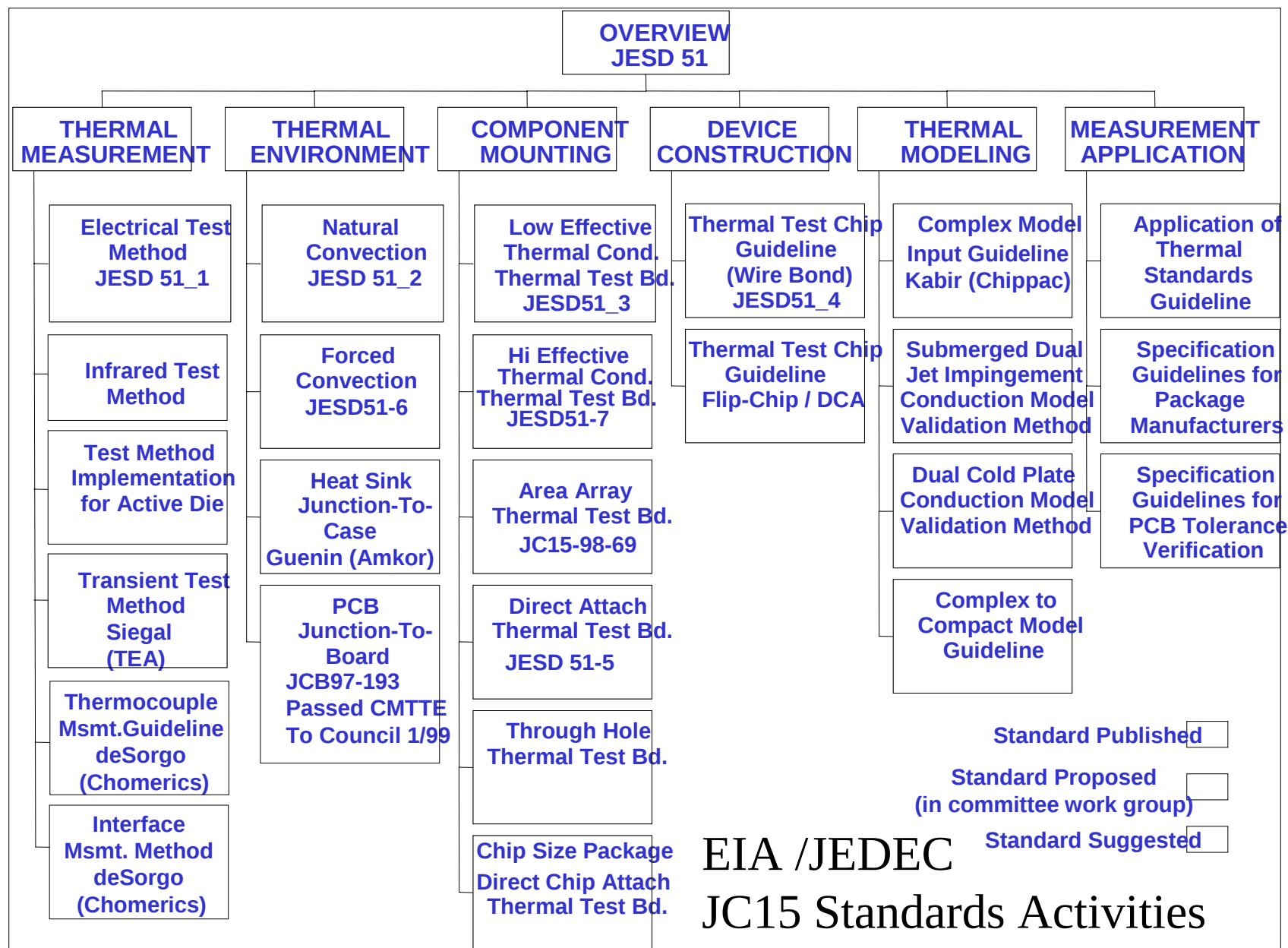


Star Model



Shunt Model

S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.



EIA /JEDEC JC15 Standards Activities

S. Shidore, Flomerics Inc.,
International Standards Committee Meeting, 1999.

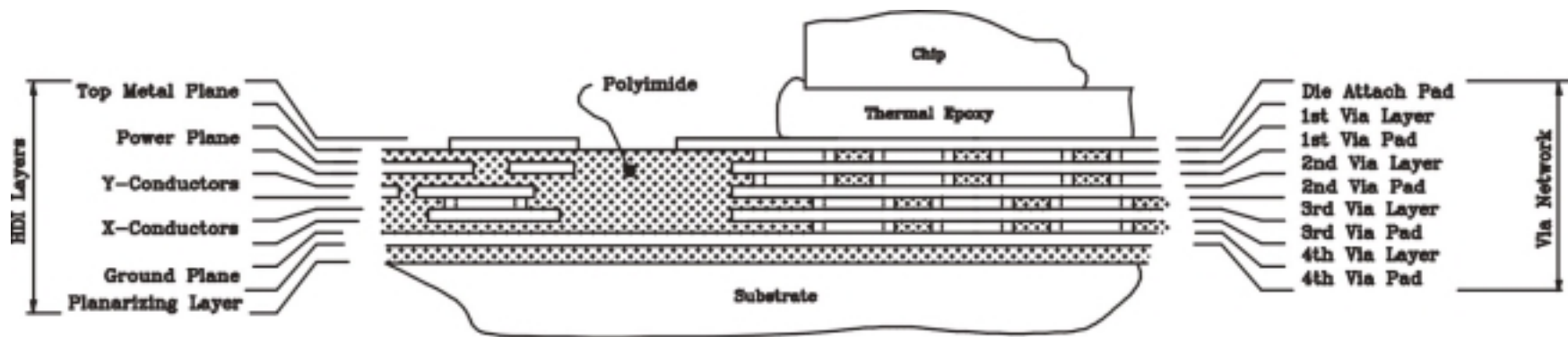
Examples of Compact Models

- Total resistance of multilayered substrates (vias)
- Natural convection in vented enclosures
- Natural convection plate fin heat sink
- Compact heat exchangers



Thermal Vias

- Analytical model for via networks
- Typical configuration of a 5-layer High Density Interconnect
- 5 copper layers separated by 5 polyimide layers

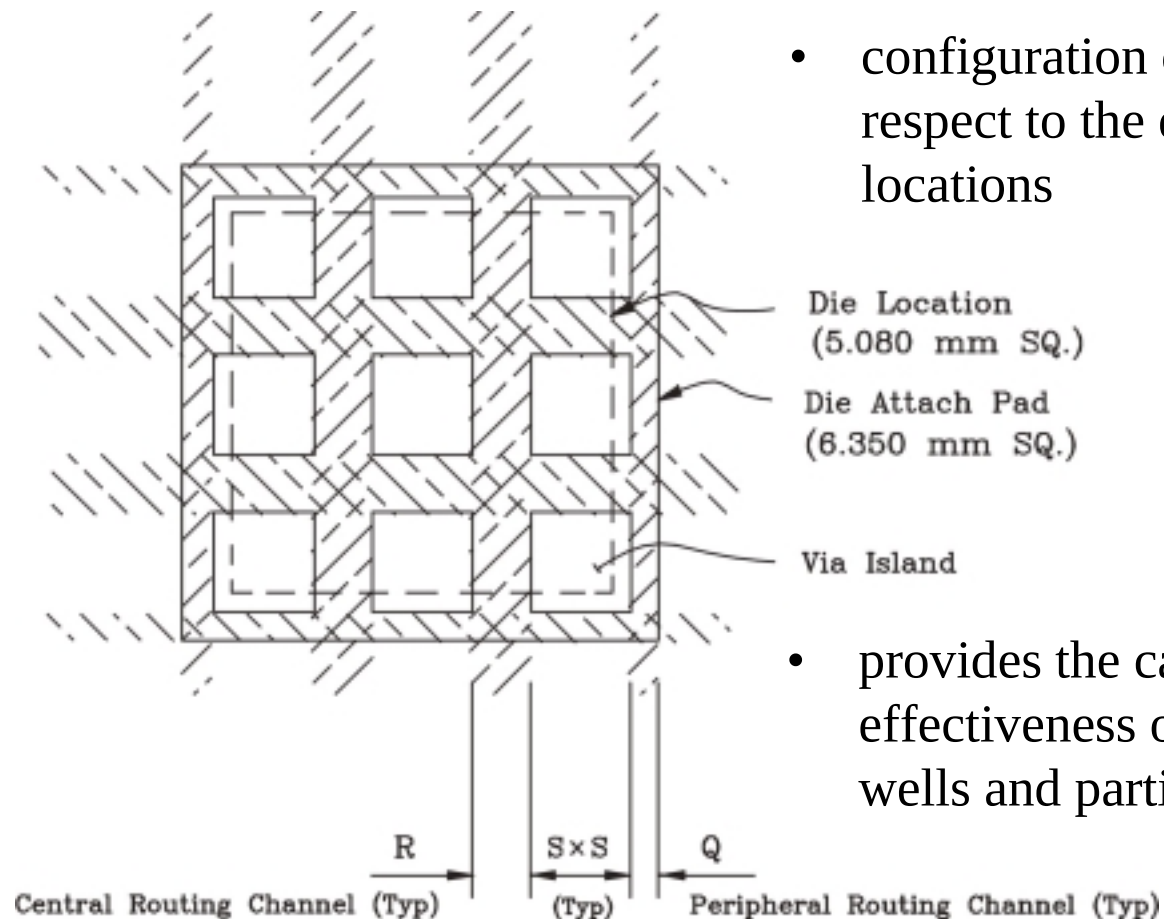


Dimensions and Thermal Conductivities

Item	Dimensions (μm)	k (W / mK)
Die	5080 x 5080 x 25	150
Thermal Epoxy	5 (thickness)	3.8
Die Attach Pad	6350 x 6350 x 5	310
Planarizing Layer	5 (thickness)	0.19
HDI Dielectric, Polyimide Layers	5 (thickness)	0.19
HDI Conductive Layers, Via Pads	5 (thickness)	386
Vias	35 O.D. x 28 I.D. x 5	386
Ceramic Substrate	1016 (thickness)	30
Grease Layer	25 (thickness)	0.8

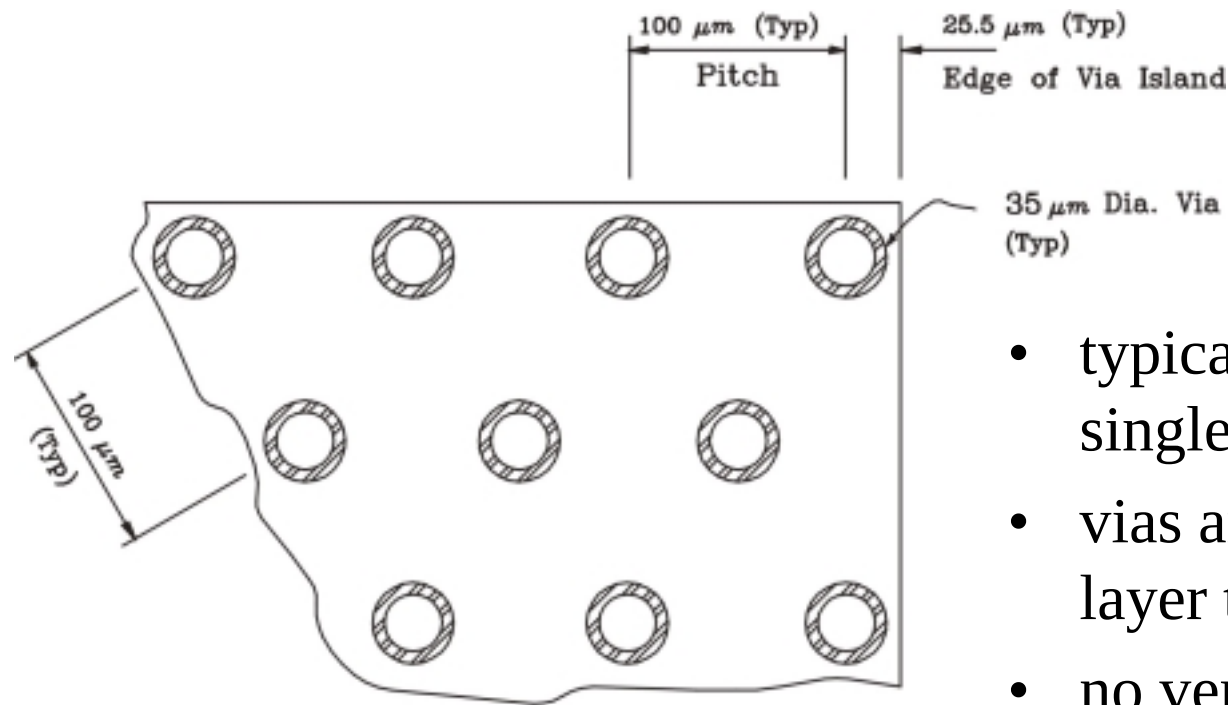


Thermal Vias



- configuration of the via island with respect to the die and the die attach pad locations
- provides the capability to compare the effectiveness of thermal vias, thermal wells and partial thermal wells

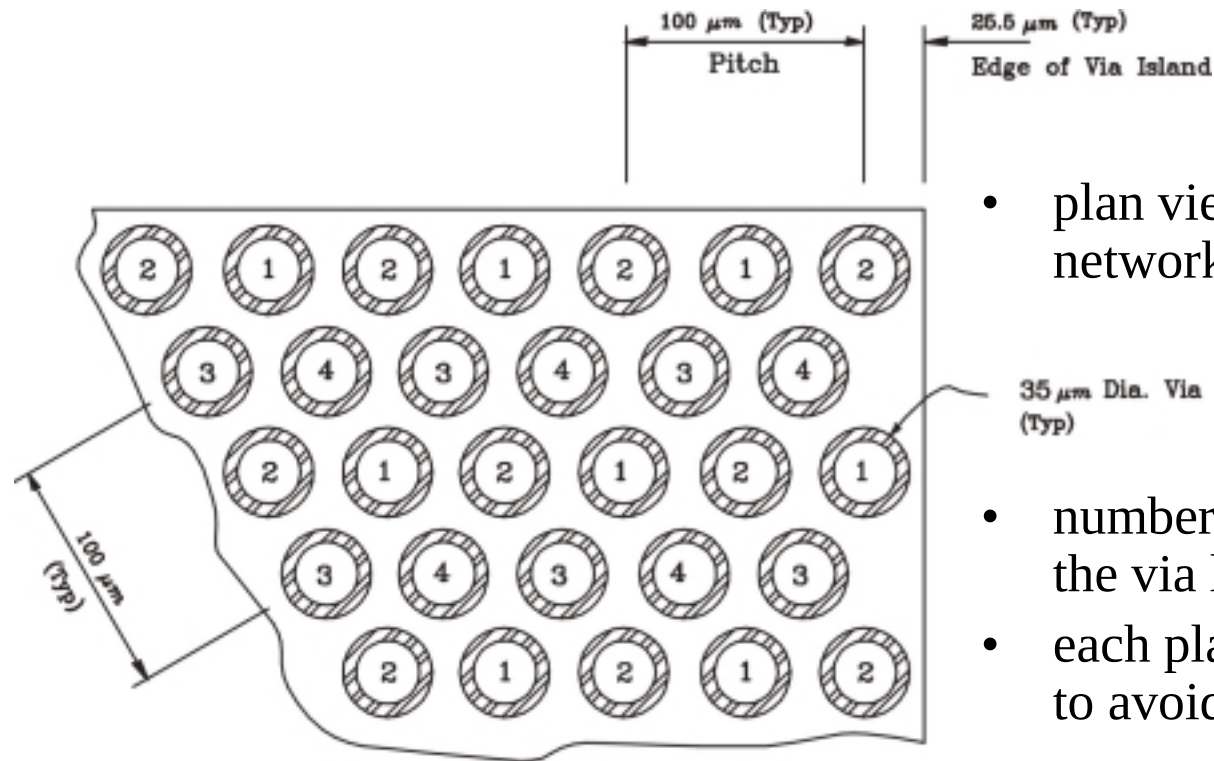
Thermal Vias



Typical section view of a via layer

- typical via layout within a single via layer
- vias are staggered from one layer to the next
- no vertical overlaps of vias occur through the layers

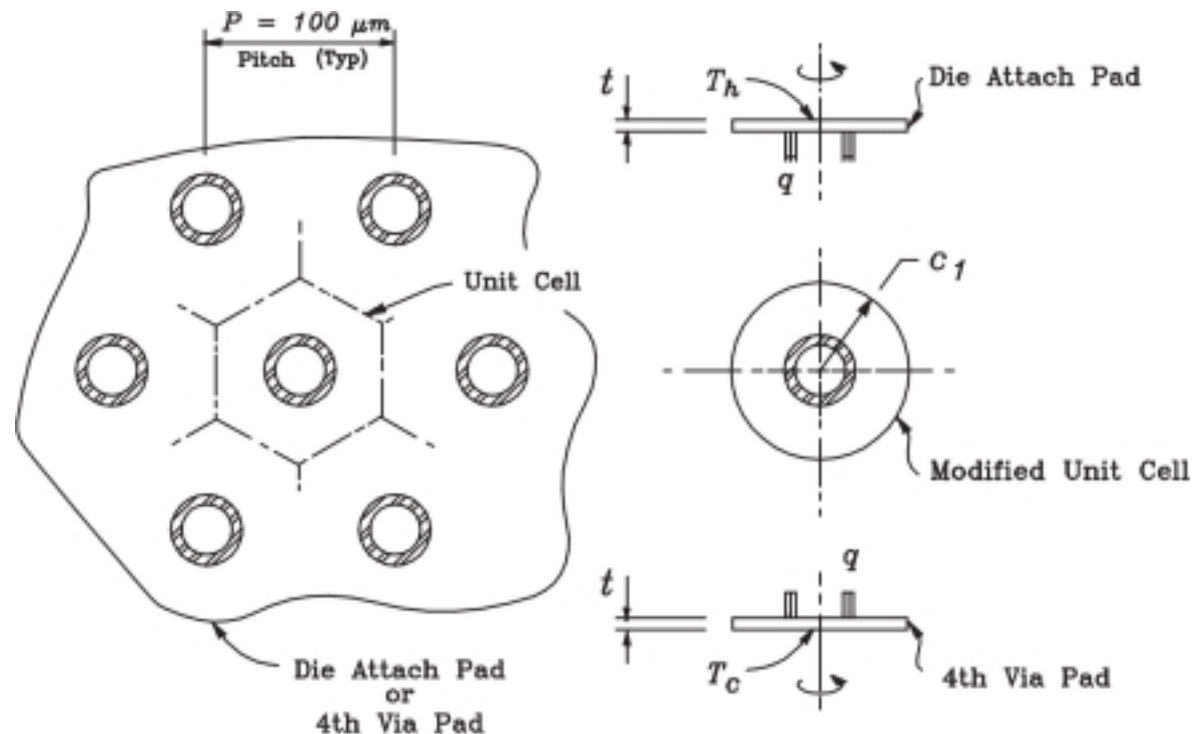
Thermal Vias



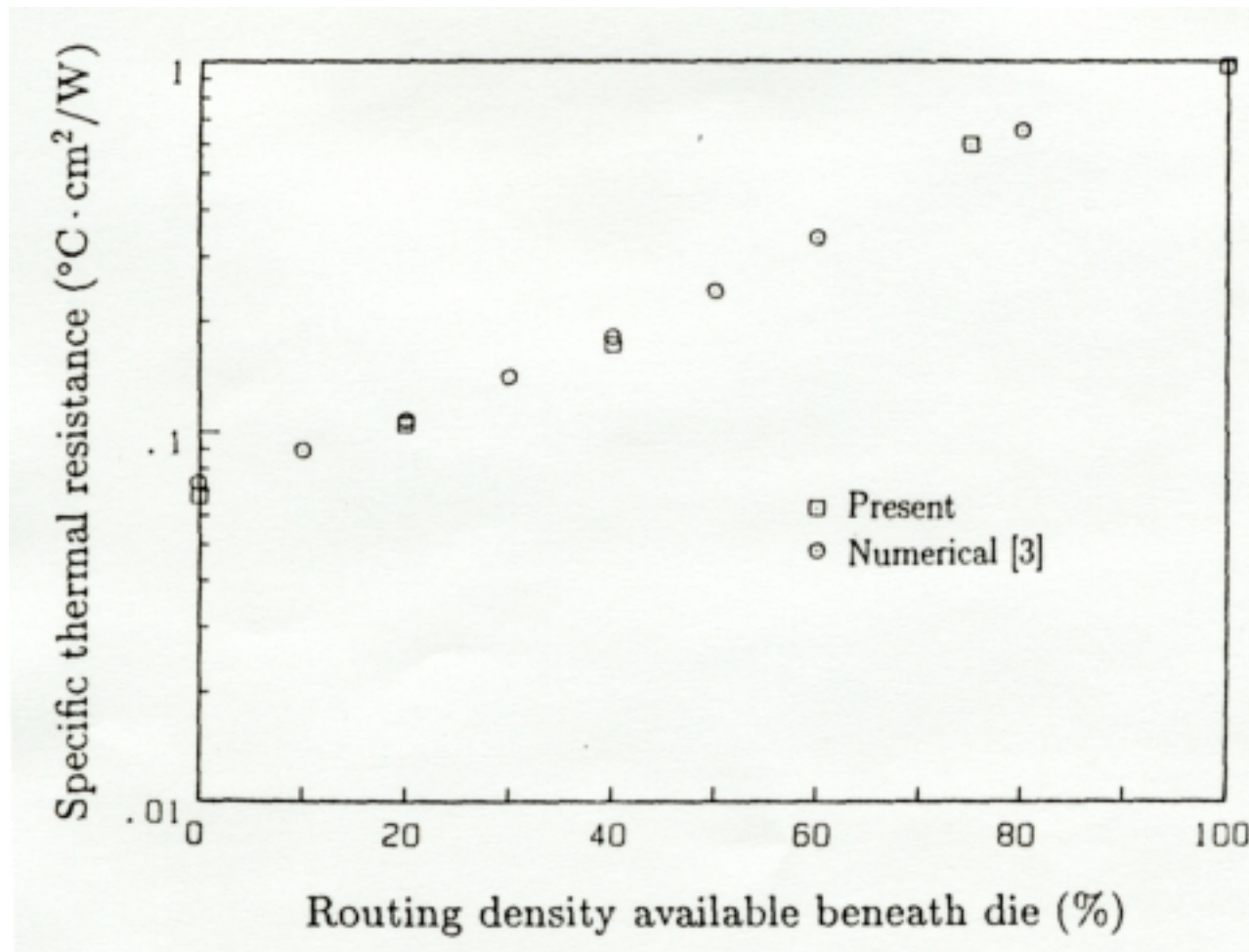
- plan view of a typical 4-layer via network
- numbers indicate the plane in which the via layer is located
- each plane has a 60 degree axis shift to avoid via overlap

Compact Model: Thermal Vias

- Isolate basic unit cell
- Model as a circular disk with an isoflux boundary



Model Validation



Natural Convection in Vented Enclosures

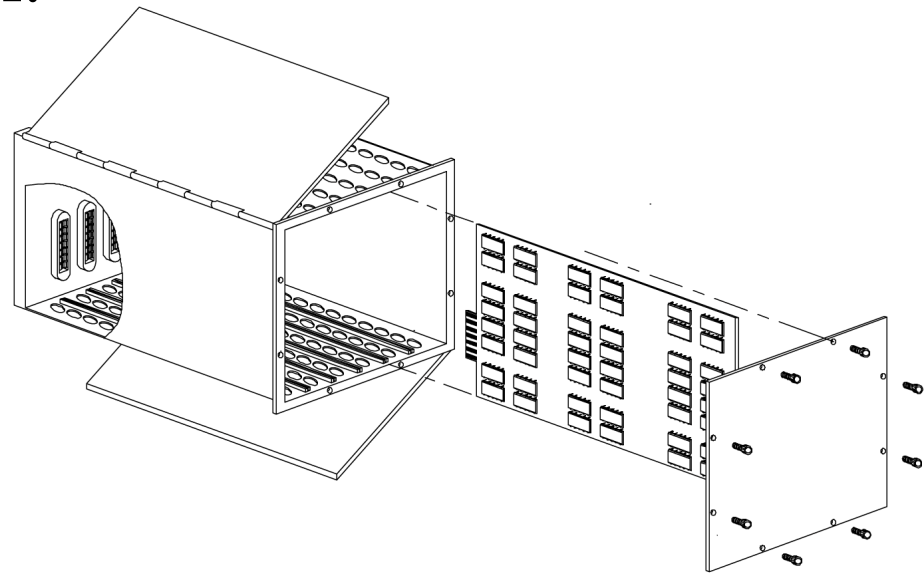
- Natural convection heat transfer for a parallel array of circuit boards in a vented enclosure
- Flow restrictions at inlet, outlet
- Solve for each channel:

$$\Delta \bar{T}_{fluid}$$

$$\bar{U}_{fluid}$$

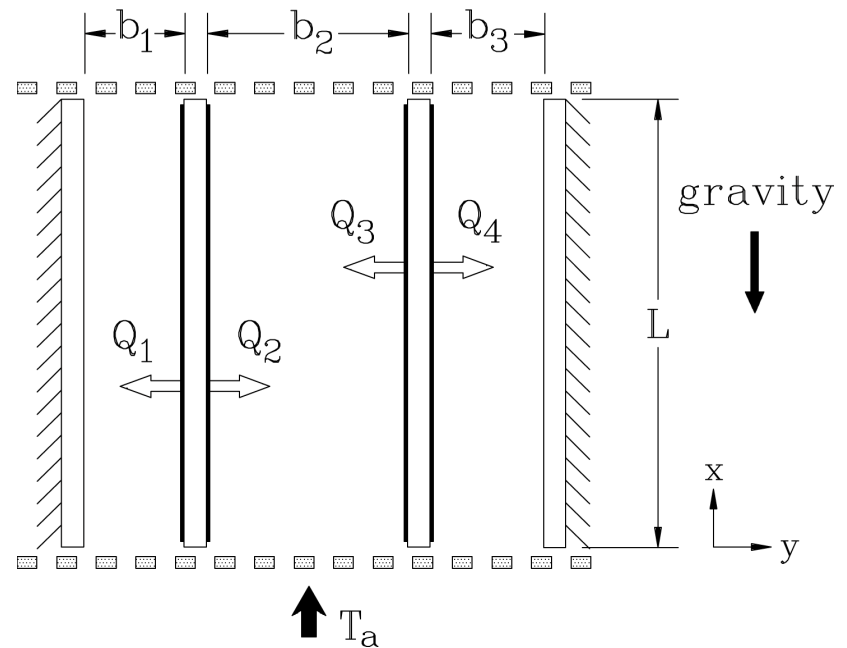
$$T_{max\ board}$$

$$Q_{1,2\ board}$$

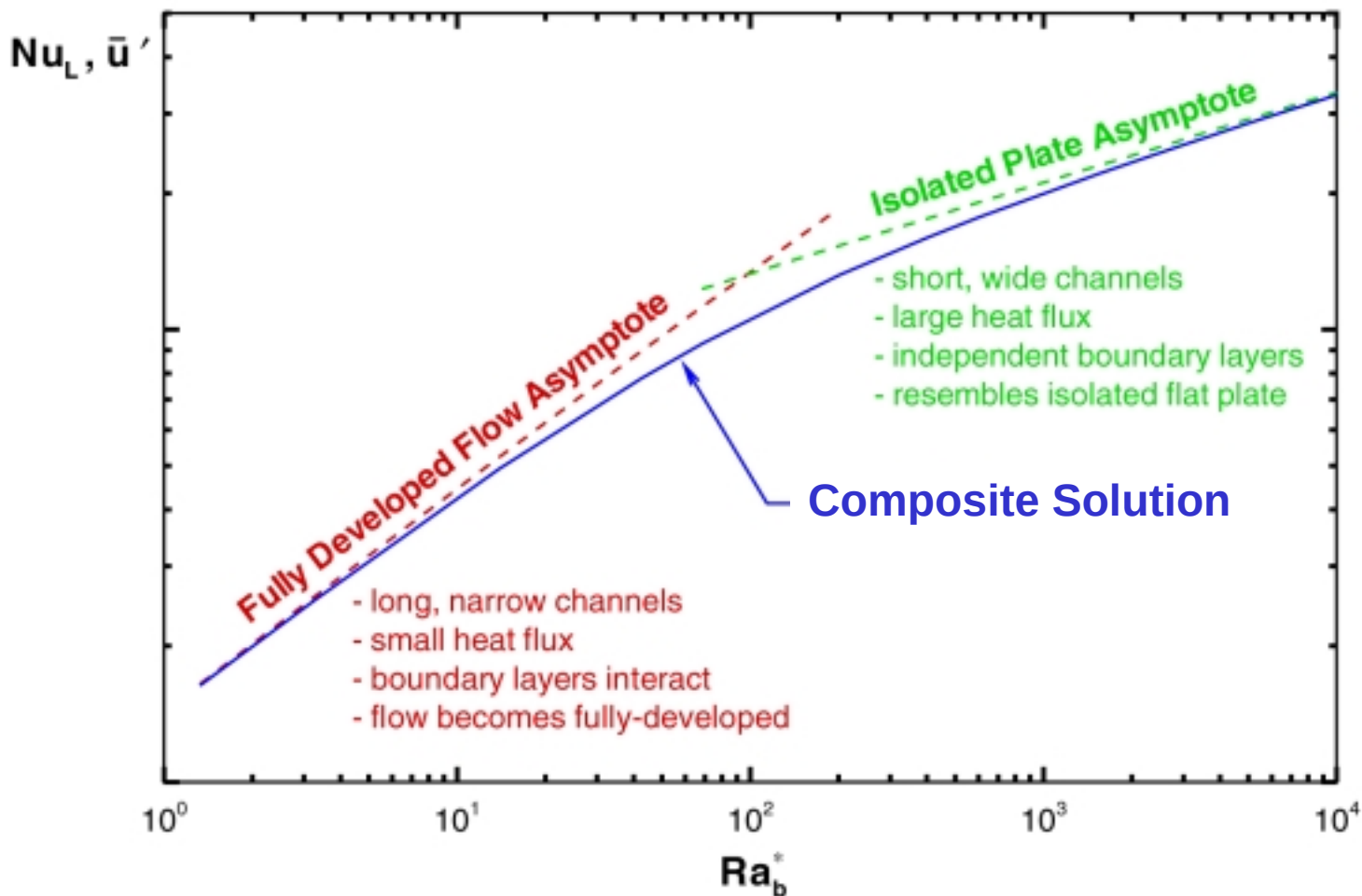


Modeling Approach

- Laminar natural convection between parallel plates
- Assumptions:
 - 2D channel flow
 - isoflux boundary conditions
 - adiabatic boundaries at outer walls
 - EMC screens at inlet, exit



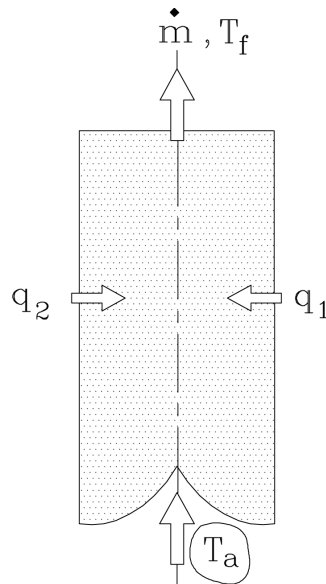
Composite Solution Procedure



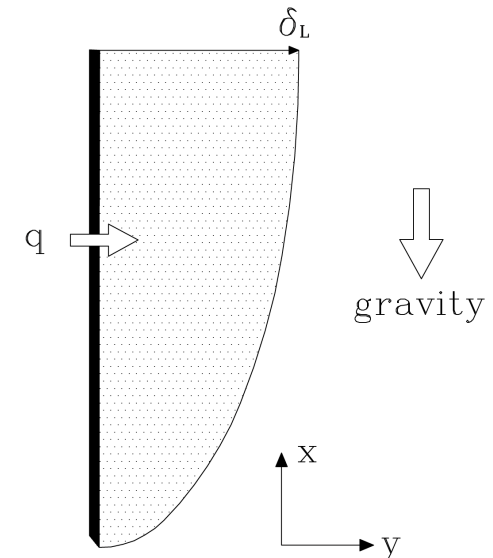
Nusselt Number

$$Nu_L = \frac{q L}{k \Delta T} = \left[(Nu_{fd})^{-n} + (Nu_{ip})^{-n} \right]^{-1/n}$$

**Fully Developed
Channel Flow**



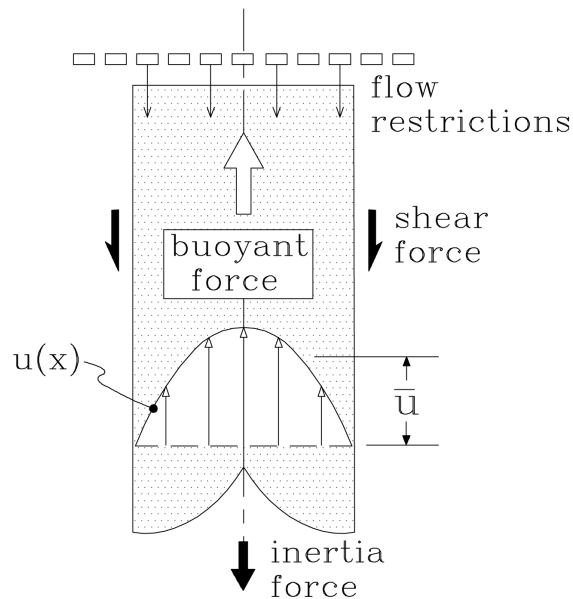
**Isolated Plate, Laminar
Boundary Layer Flow**



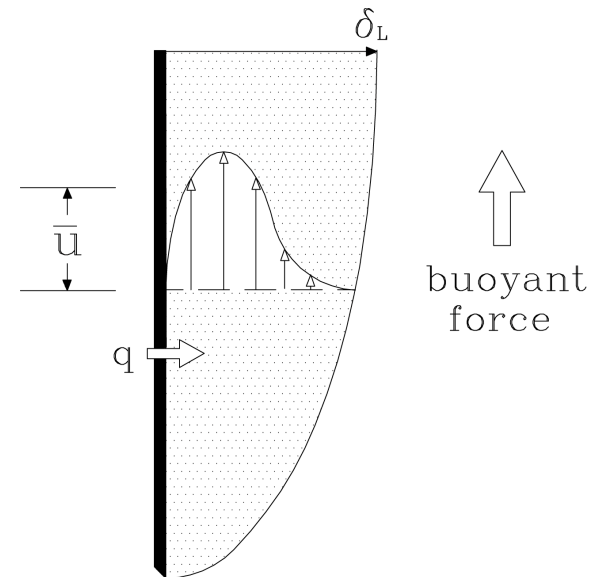
Mean Velocity

$$Re_b = \frac{\bar{U} b}{\nu} = \left[\left(Re_{fd} \right)^{-n} + \left(Re_{ip} \right)^{-n} \right]^{-1/n}$$

**Fully Developed
Channel Flow**



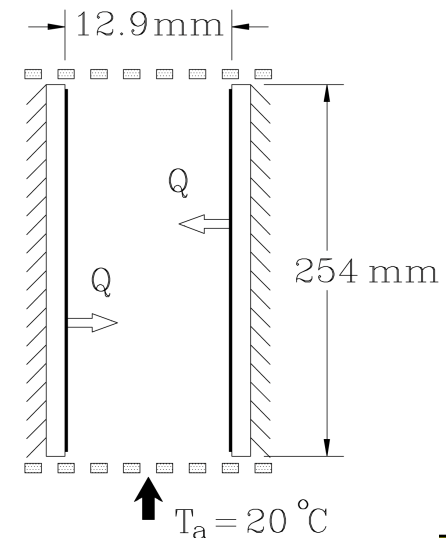
**Isolated Plate, Laminar
Boundary Layer Flow**



Model Validation

Q (W / side)	% open	K	Model		Exp. Data	
			ΔT_{board} (°C)	ΔT_{fluid} (°C)	ΔT_{board} (°C)	ΔT_{fluid} (°C)
5.25	100	0	22.5	15.7	22.2	14.7
5.25	62.8	4.3	25.0	20.1	26.4	18.5
4.0	49.2	8.2	22.2	19.2	23.5	18.0
4.0	38.4	14.8	24.4	22.0	26.9	21.1

- Symmetrically heated, single channel
- EMC screens at inlet, outlet



Air Cooled Electronic Heat Sinks

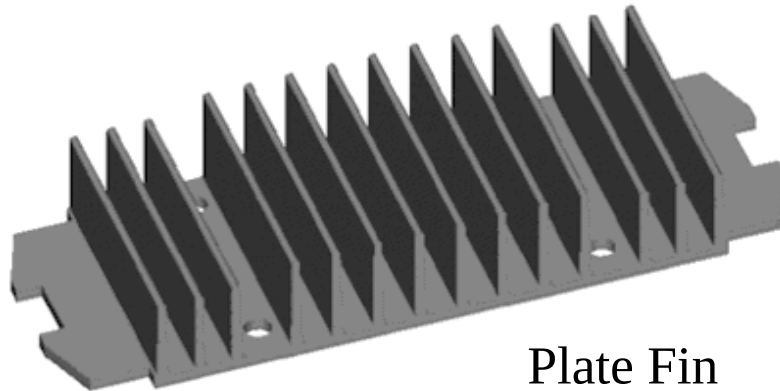
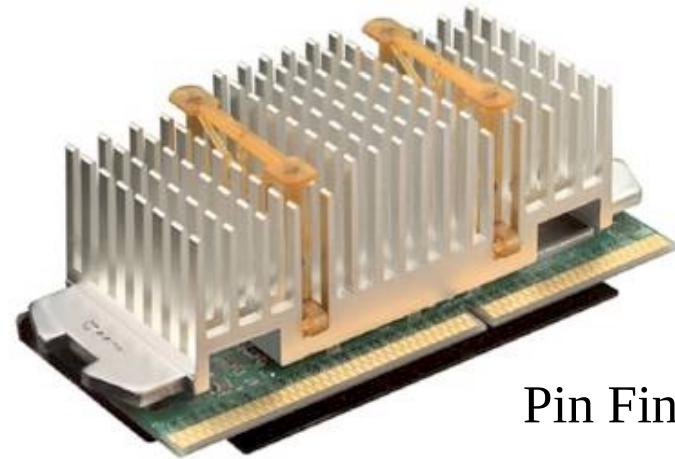
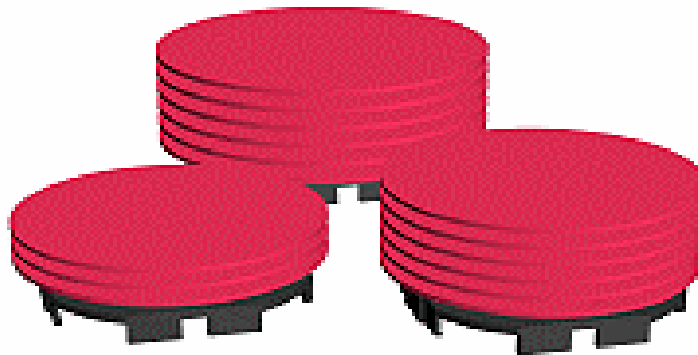


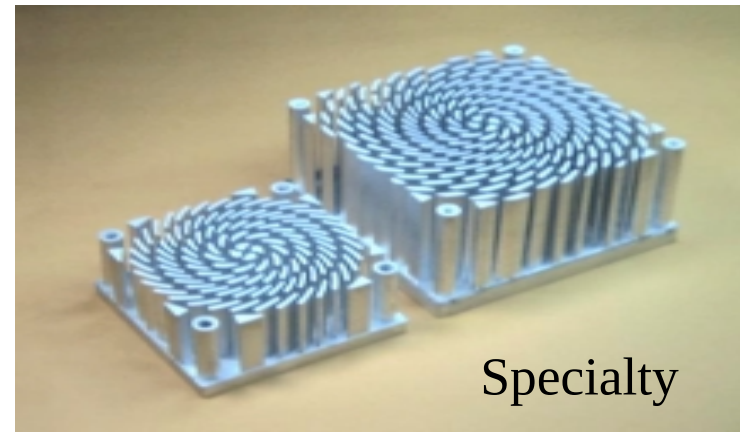
Plate Fin



Pin Fin

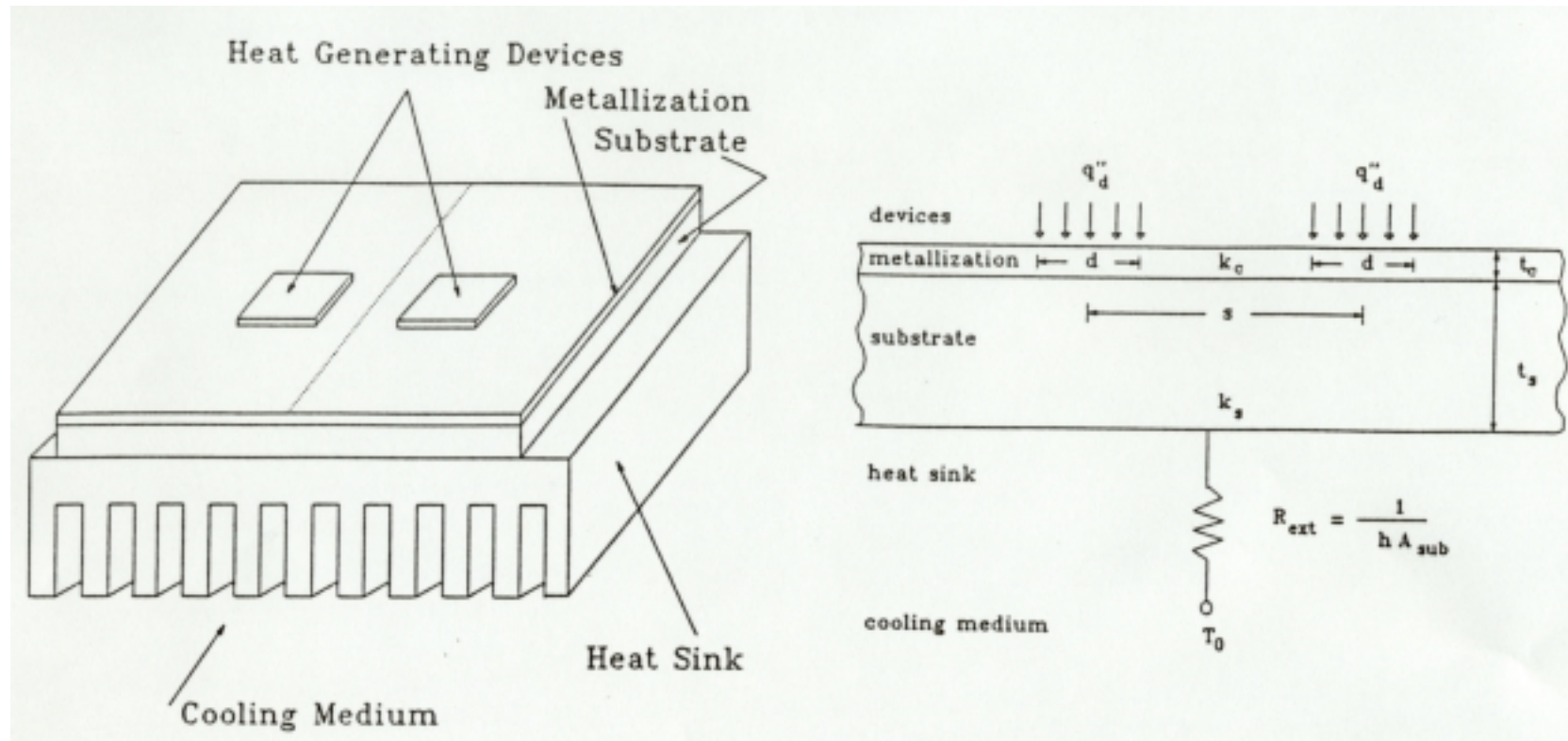


Radial Fin



Specialty

Microelectronics Heat Sink Application



M. M. Hussein et al., IEEE Semitherm Symposium, 1991, pp. 117 - 122.

Compact Model

$$Nu = \underbrace{Nu_0}_{\text{diffusion}} + \frac{1}{\underbrace{\left[\left(\frac{1}{Nu_2} \right)^2 + \left(\frac{1}{Nu_3 + Nu_4} \right)^2 \right]^{-1/2}}_{\text{channel flow}}} + \underbrace{Nu_1}_{\text{external boundary layer flow}}$$

diffusion + channel flow + external boundary layer flow

Compact Modeling Procedure

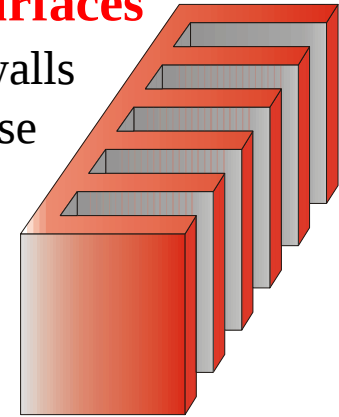
Given: dimensions & temperature

Find: Nu_b vs. $Ra_b \rightarrow = \frac{g\beta\Delta T b^3}{\alpha\nu} \cdot \frac{b}{L}$

$\hookrightarrow = \frac{hb}{k_f}$

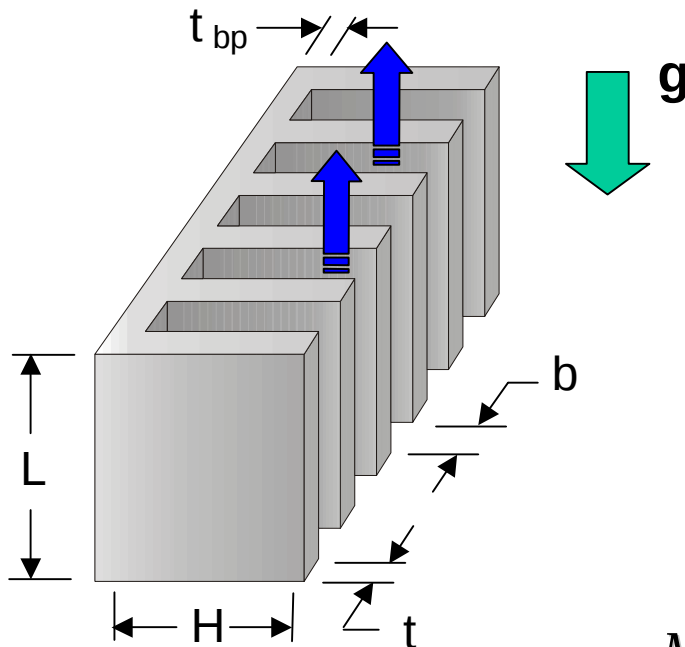
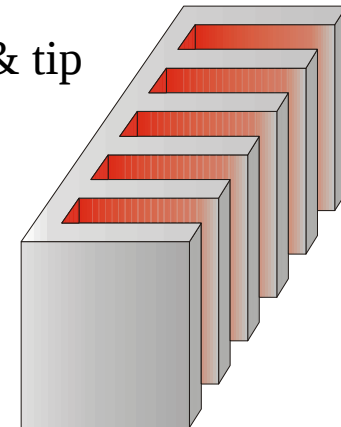
Interior Surfaces

- fins: side walls
- channel base

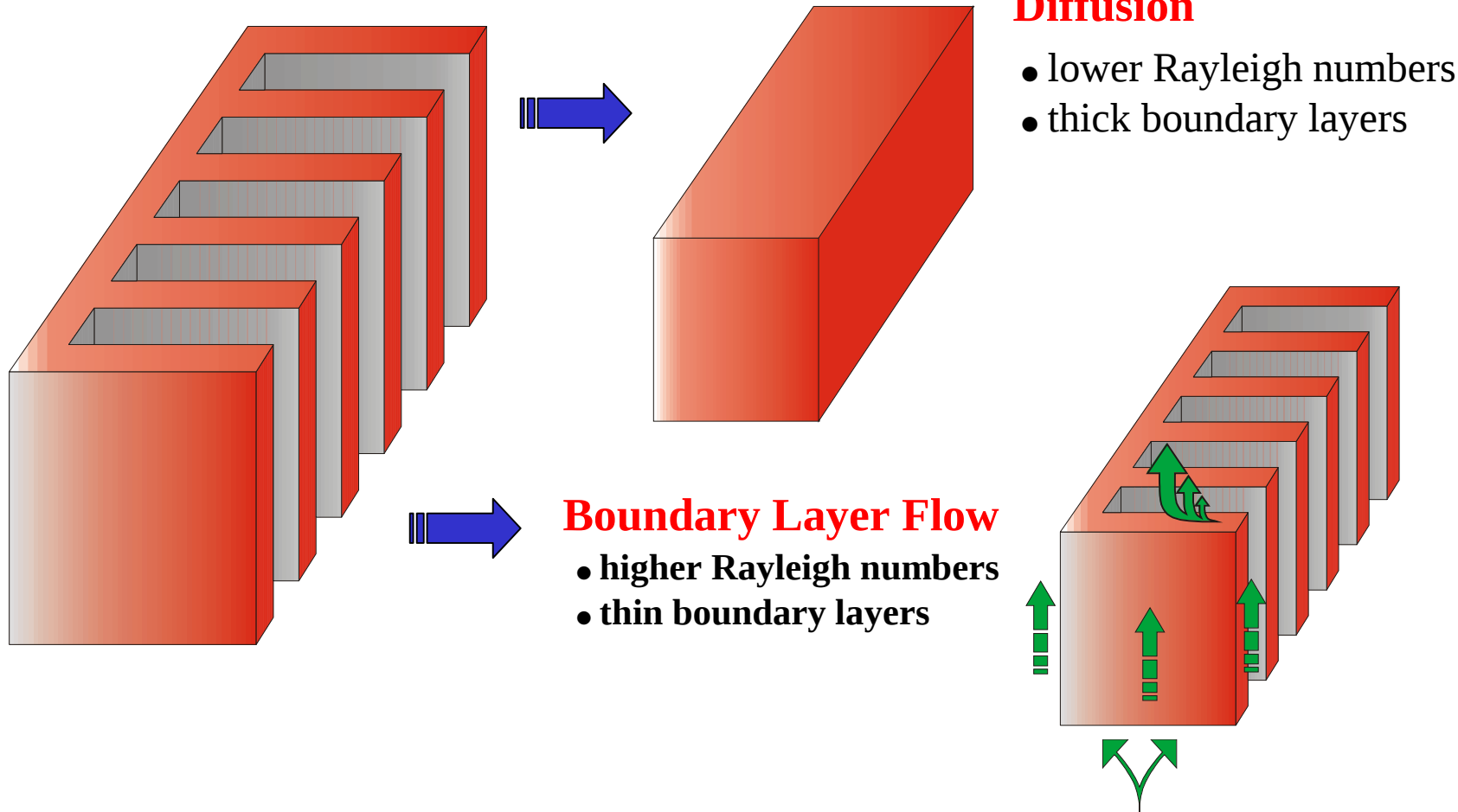


Exterior Surfaces

- fins: top, bottom, ends & tip
- base plate: top, bottom, ends and back



Exterior Surfaces



Diffusion Model

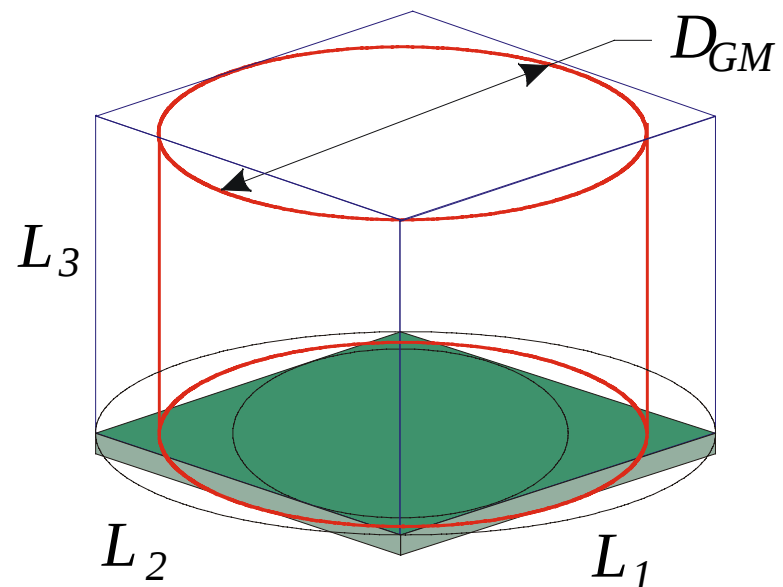
$$Nu_0 = S_{\sqrt{A}}^* = \left(S_{\sqrt{A}}^* \right)_{plate} \left(\frac{1 + 0.8688 (L_3/D_{GM})^{0.76}}{\sqrt{1 + 2L_3/D_{GM}}} \right)$$

$$1.0 \leq L_1/L_2 \leq 5.0$$

$$\left(S_{\sqrt{A}}^* \right)_{plate} = \frac{\sqrt{2/\pi} \left(1 + \sqrt{L_1/L_2} \right)^2}{\sqrt{L_1/L_2}}$$

$$5.0 < L_1/L_2 < \infty$$

$$\left(S_{\sqrt{A}}^* \right)_{plate} = \frac{2\sqrt{2\pi}\sqrt{L_1/L_2}}{\ln(4L_1/L_2)}$$



Parallel Plates Models

- Elenbaas, 1941

$$Nu_b = \frac{1}{24} Ra_b \left[1 - \exp(-35/Ra_b) \right]^{3/4}$$

- Churchill, 1977

$$Nu_b = \left[Nu_{fd}^{-m} + Nu_{dev}^{-m} \right]^{-1/m}$$

$$m = 2$$

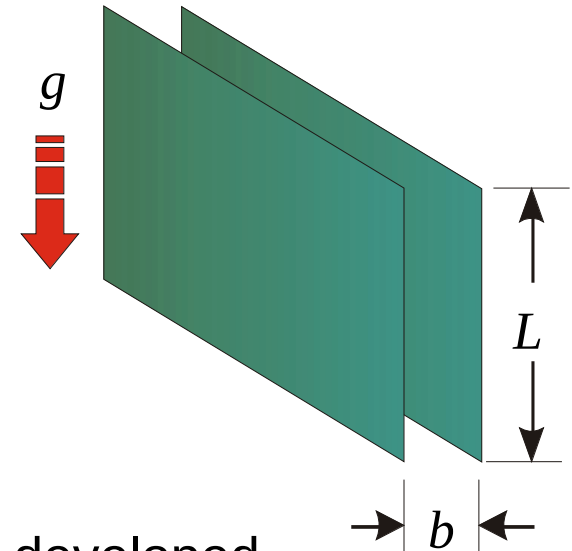
$$Nu_{fd} = \frac{1}{24} Ra_b$$

$$Nu_{dev} = G_{\sqrt{A}} \cdot F(Pr) \cdot Ra_b^{1/4}$$

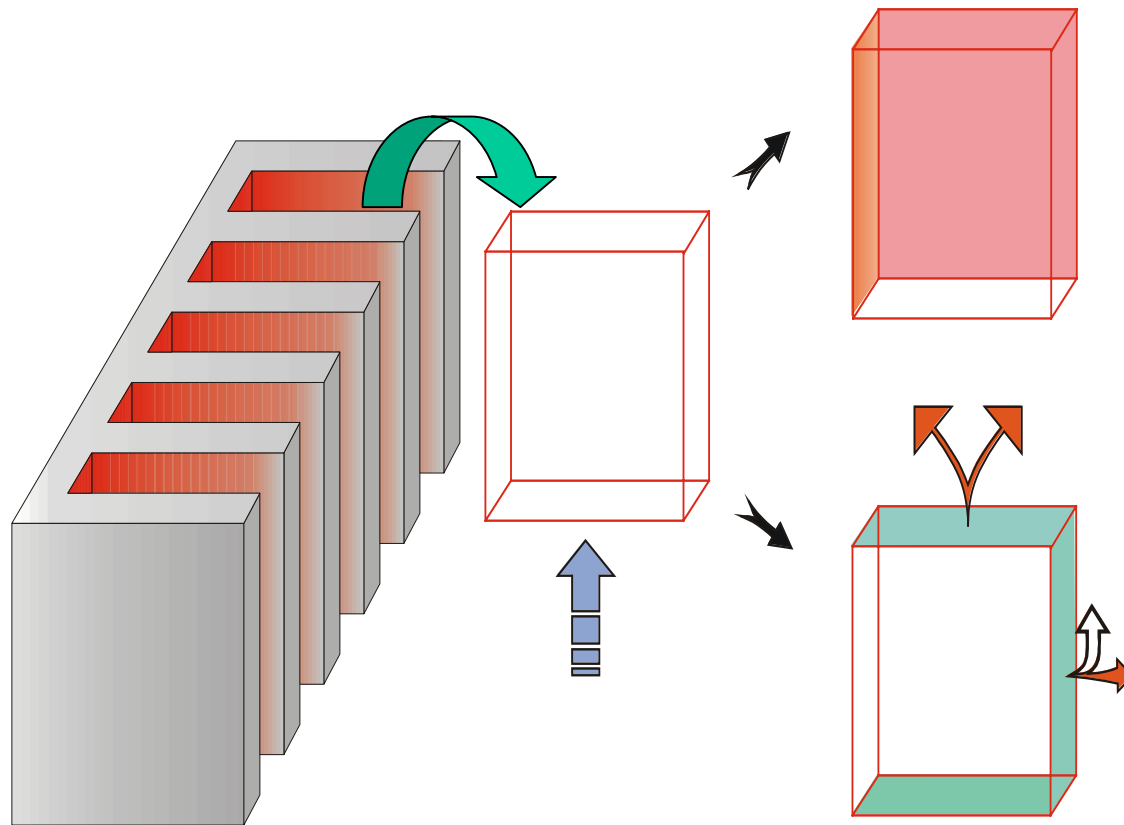
fd - fully developed
dev - developing flow

$G_{\sqrt{A}}$ - body gravity function

$F(Pr)$ - Prandtl number function



Interior Surfaces



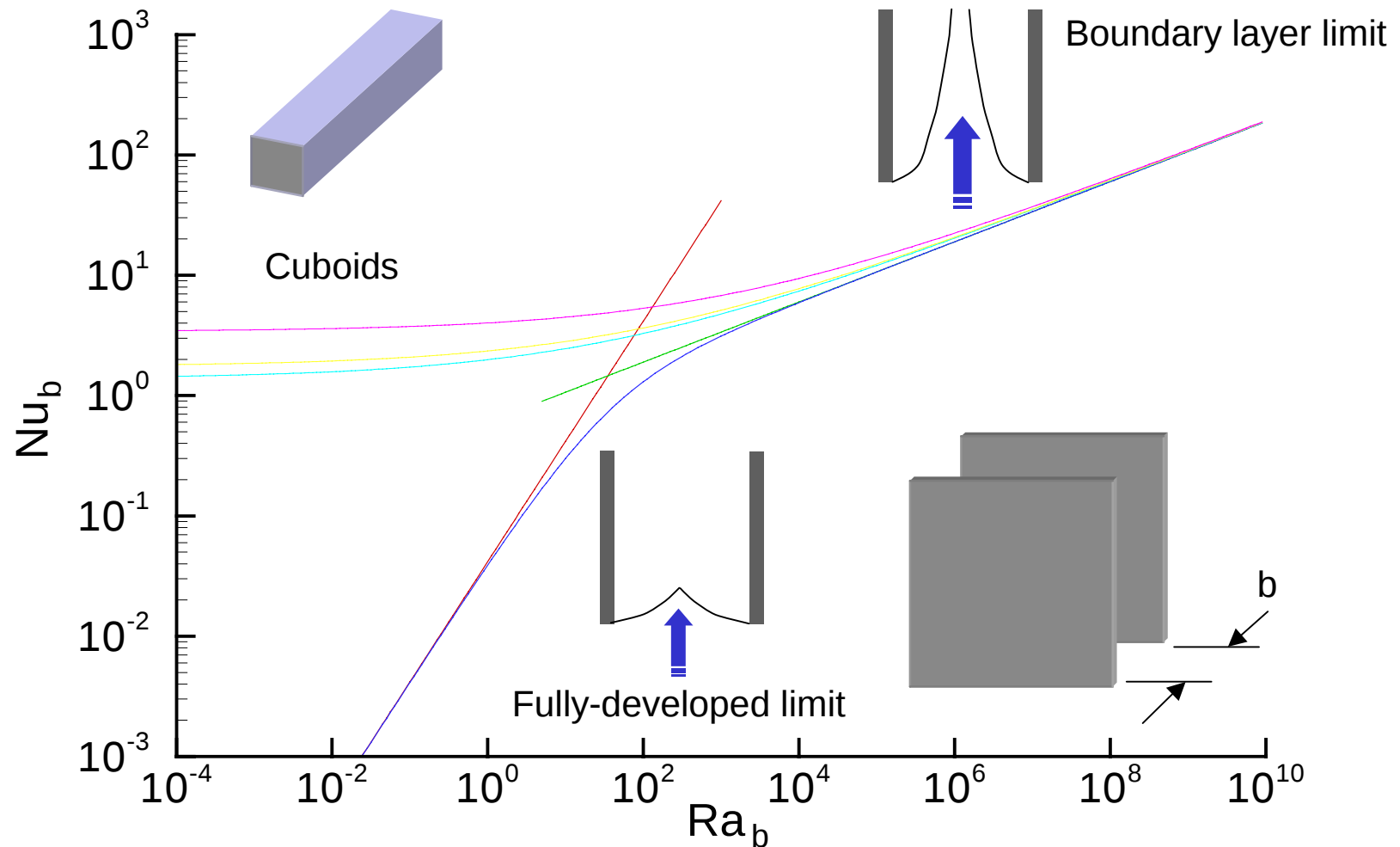
Channel Flow

- Elenbaas model with adjustment for end wall
- combined flow: developing + fully developed

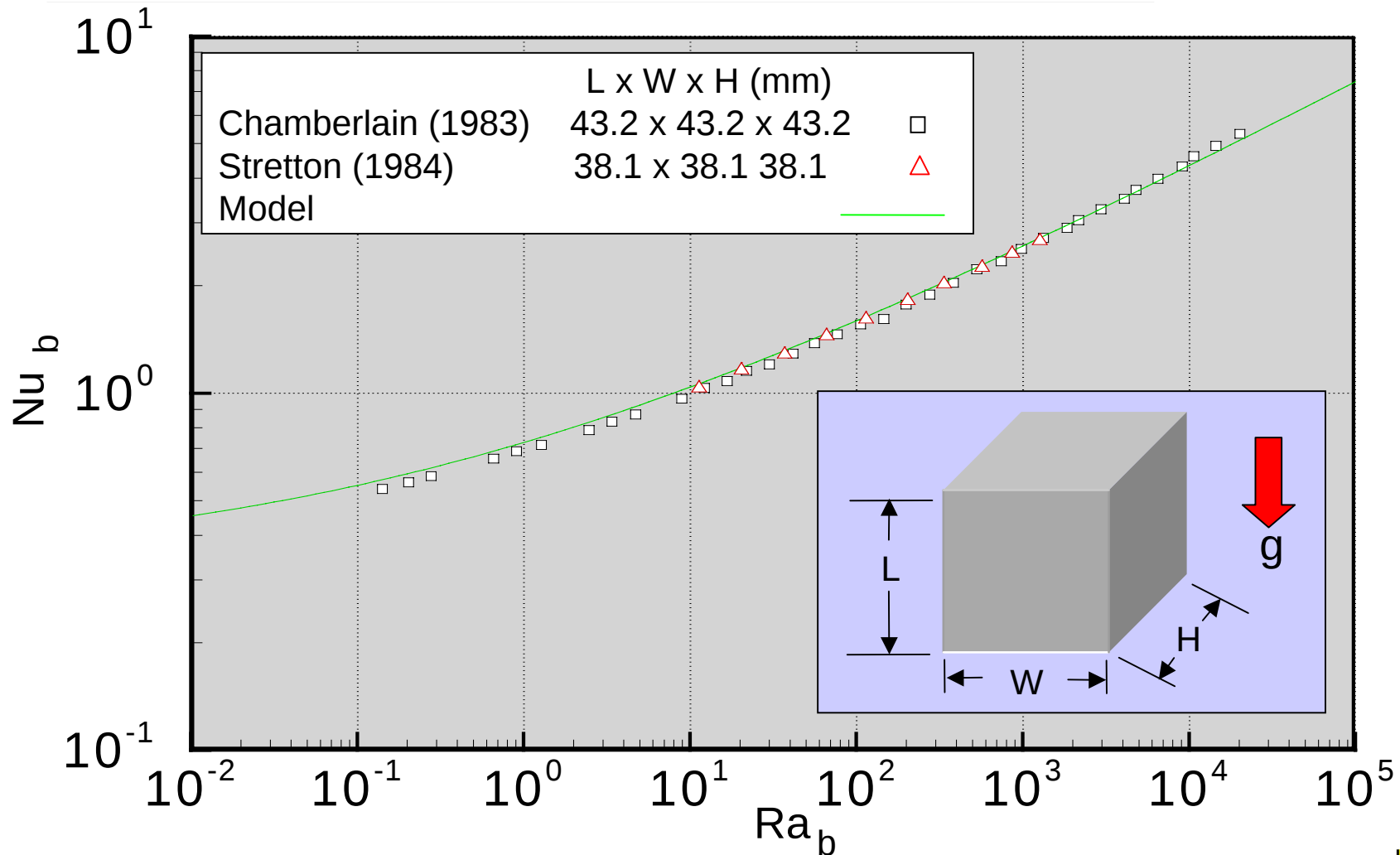
Control Surface

- open surfaces with energy migration

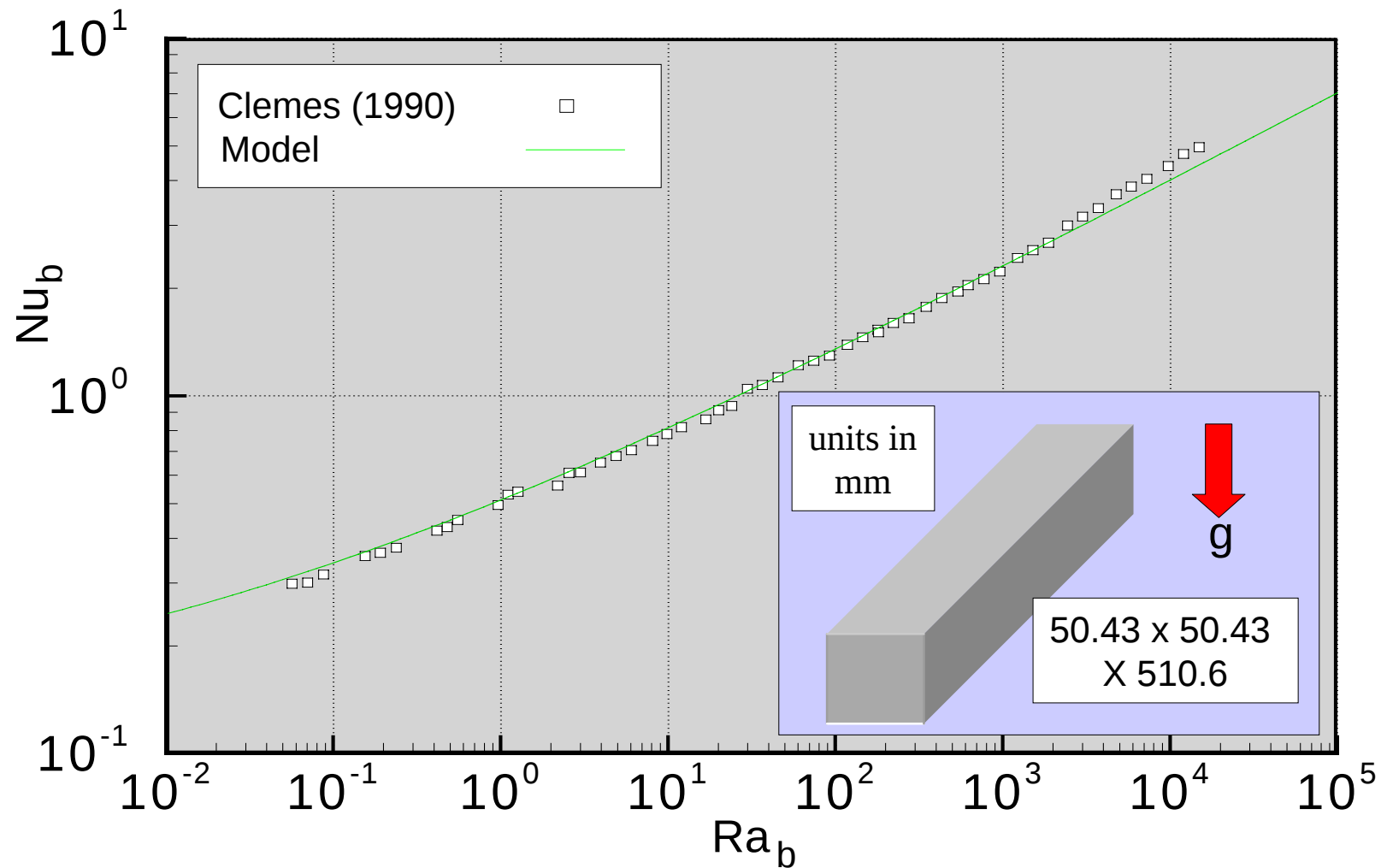
Compact Model Limiting Cases



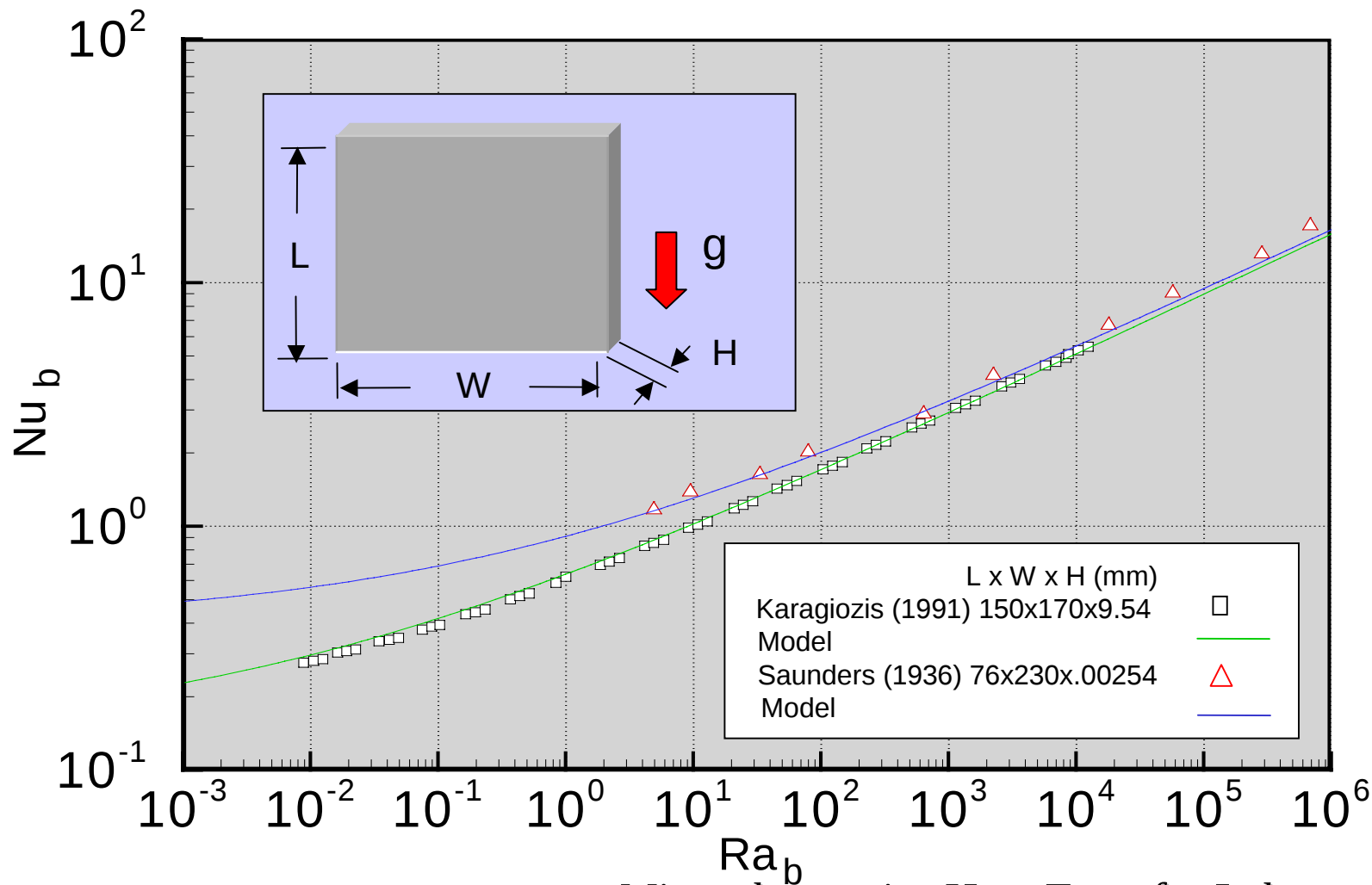
Model Validation: Cube



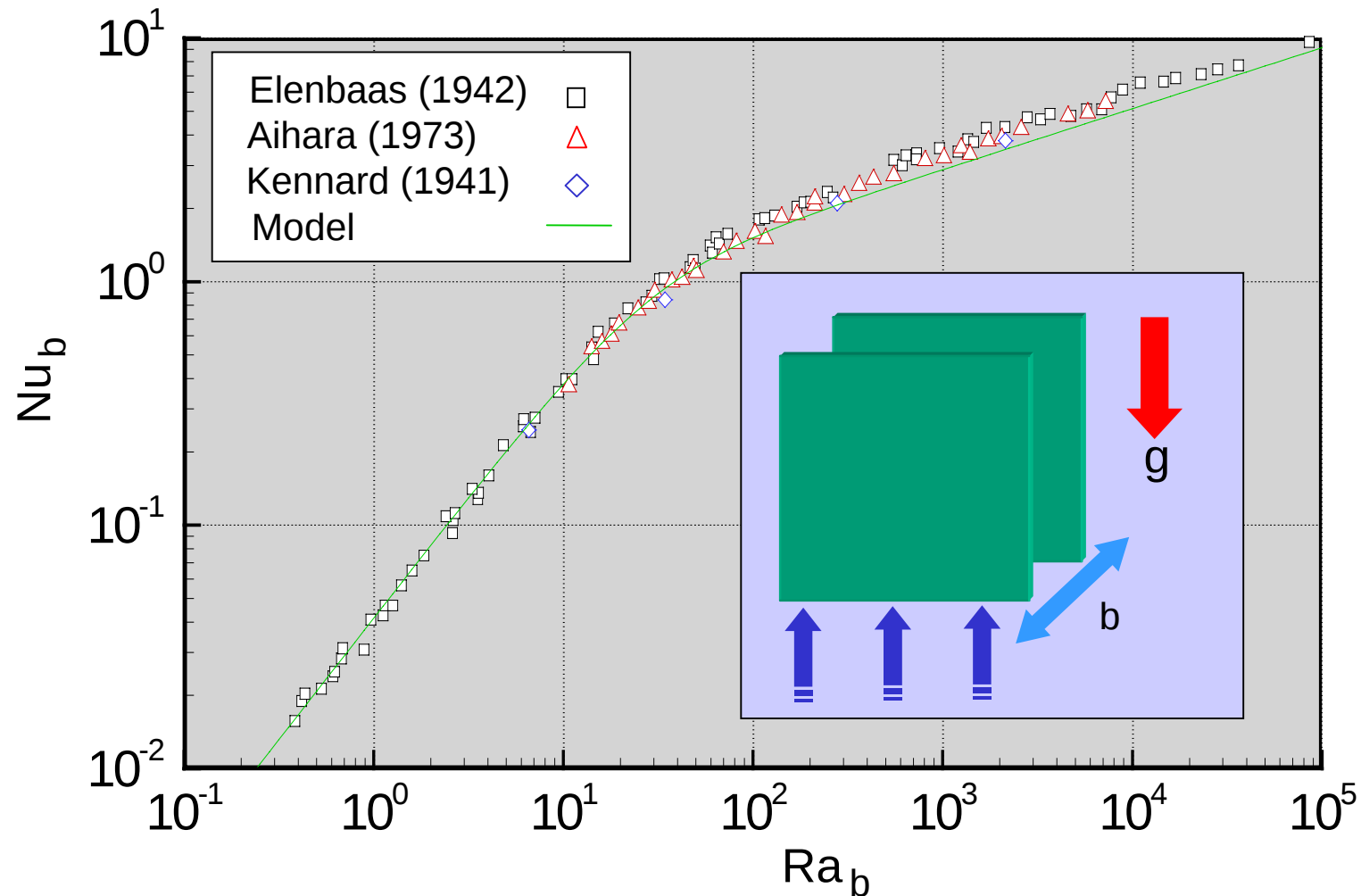
Model Validation: Cuboid



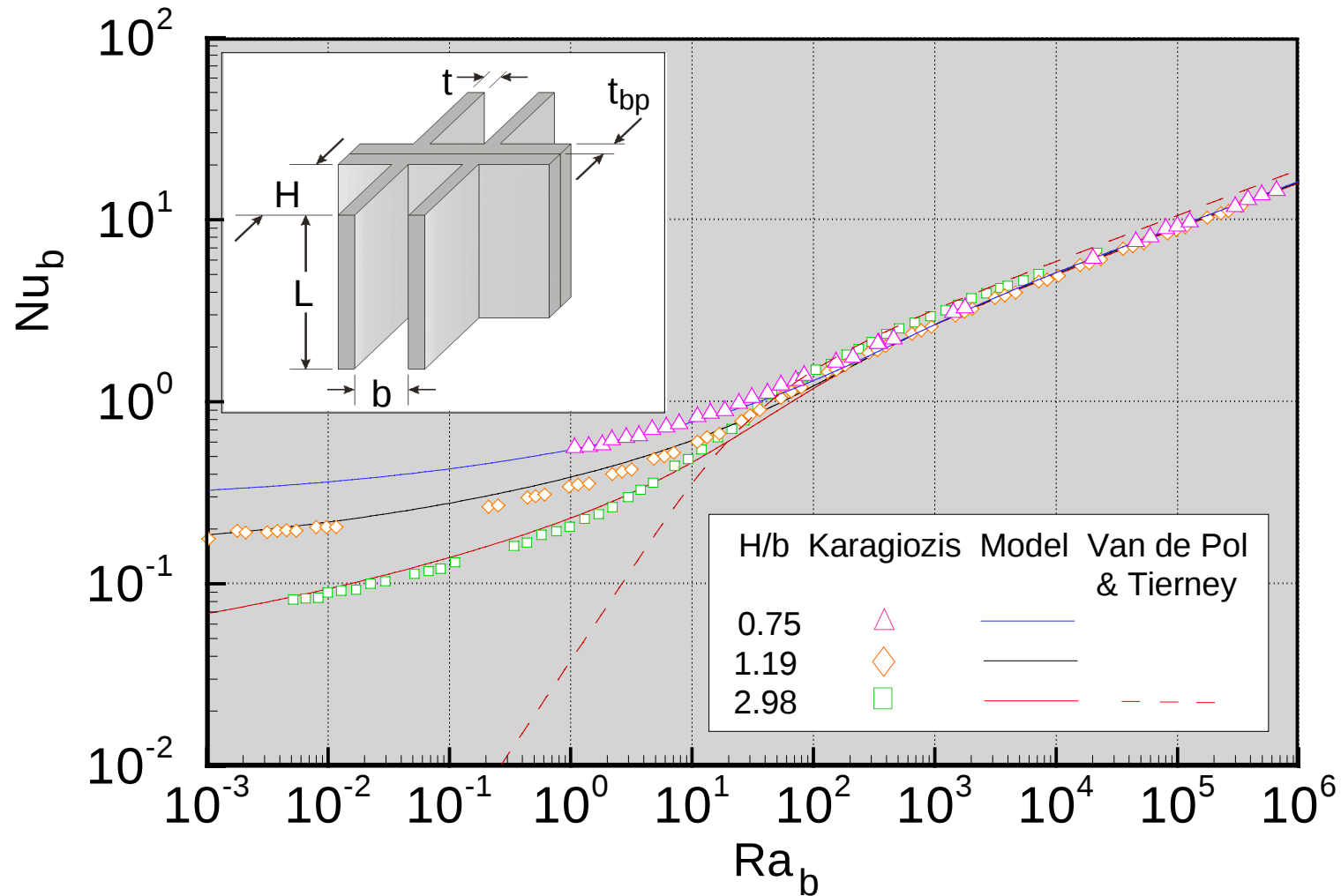
Model Validation: Vertical Plate



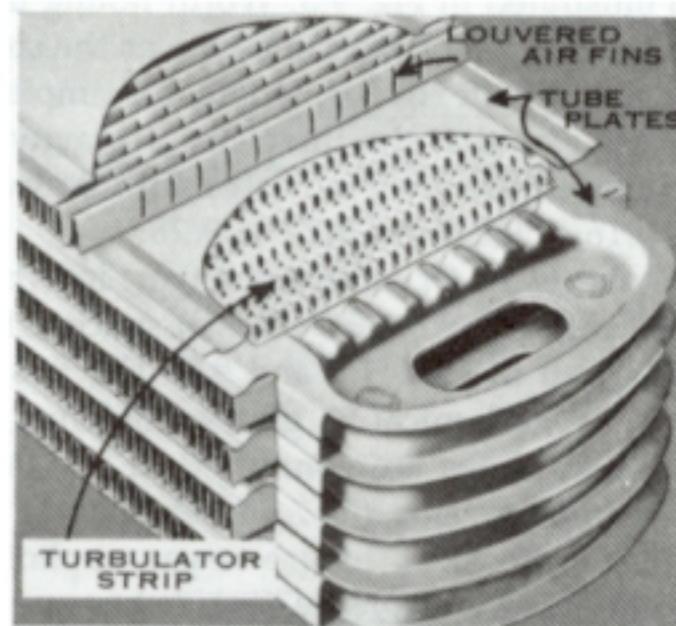
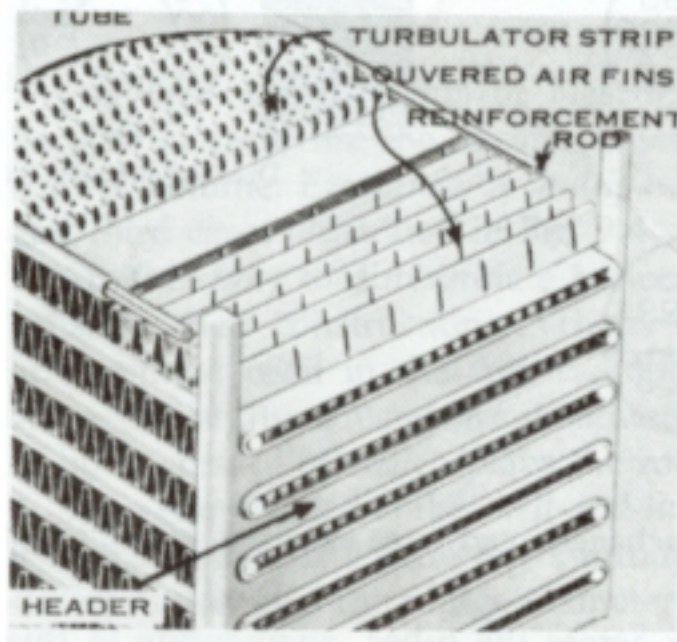
Model Validation: Parallel Plates



Model Validation: Plate Fin Heat Sinks



Automotive Heat Exchangers

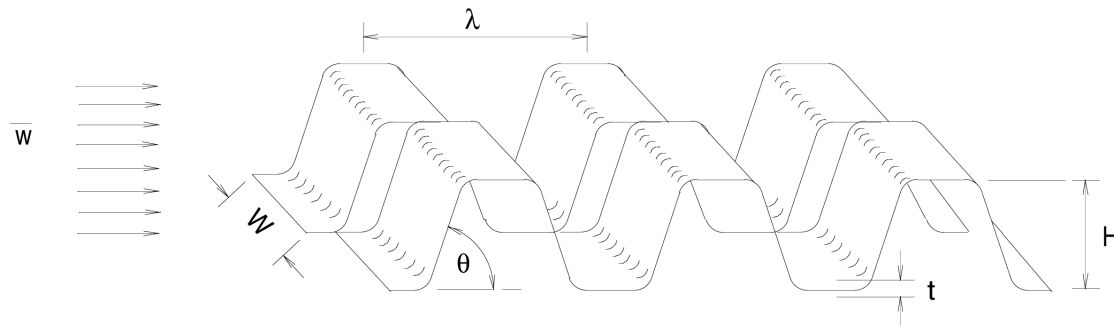


A. Bejan, Heat Transfer,
Wiley, New York, 1993.

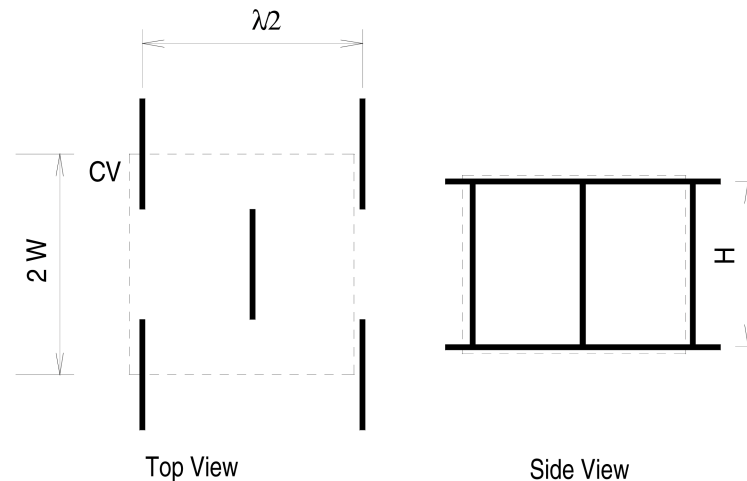
- Forced convection, internal flow
- Solve for $(\Delta P, \dot{m})$ and $(\Delta T, Q)$
- Requires f and j for wide range of Re , Pr



System Geometry and Basic Cell



Typical Turbulator Strip Geometry



Unit Cell for Compact Model

Modeling Procedure

- Define system, sub-system and basic cell
- Derive force and energy balances for basic cell
- Develop models for three flow regimes:
 - low Reynolds number (creeping) flow
 - laminar flow
 - turbulent flow
- Combine models using composite solution, valid for full range of Re
- Quantify combination parameters using experimental data

Modeling Approach

- Force balance

$$F_{total} = F_{friction} + F_{drag} + F_{losses}$$

$$\bar{f} = \frac{\bar{\tau}}{\frac{1}{2}\rho\bar{U}^2} = f(\dots) + C_D(\dots) + K(\dots)$$

where $(\dots)$ = geometry from basic cell

- Energy balance

$$Q_{total} = Q_{fins} + Q_{walls}$$

$$\bar{j} = \frac{Nu}{Re Pr^{1/3}} = j_{fins}(\dots) + j_{walls}(\dots)$$



Modeling Approach

- General form based on composite solution

$$f, j = \left[\left\{ (y_{cf})^m + (y_{lam})^m \right\}^{n/m} + (y_{tur})^n \right]^{1/n}$$

where:

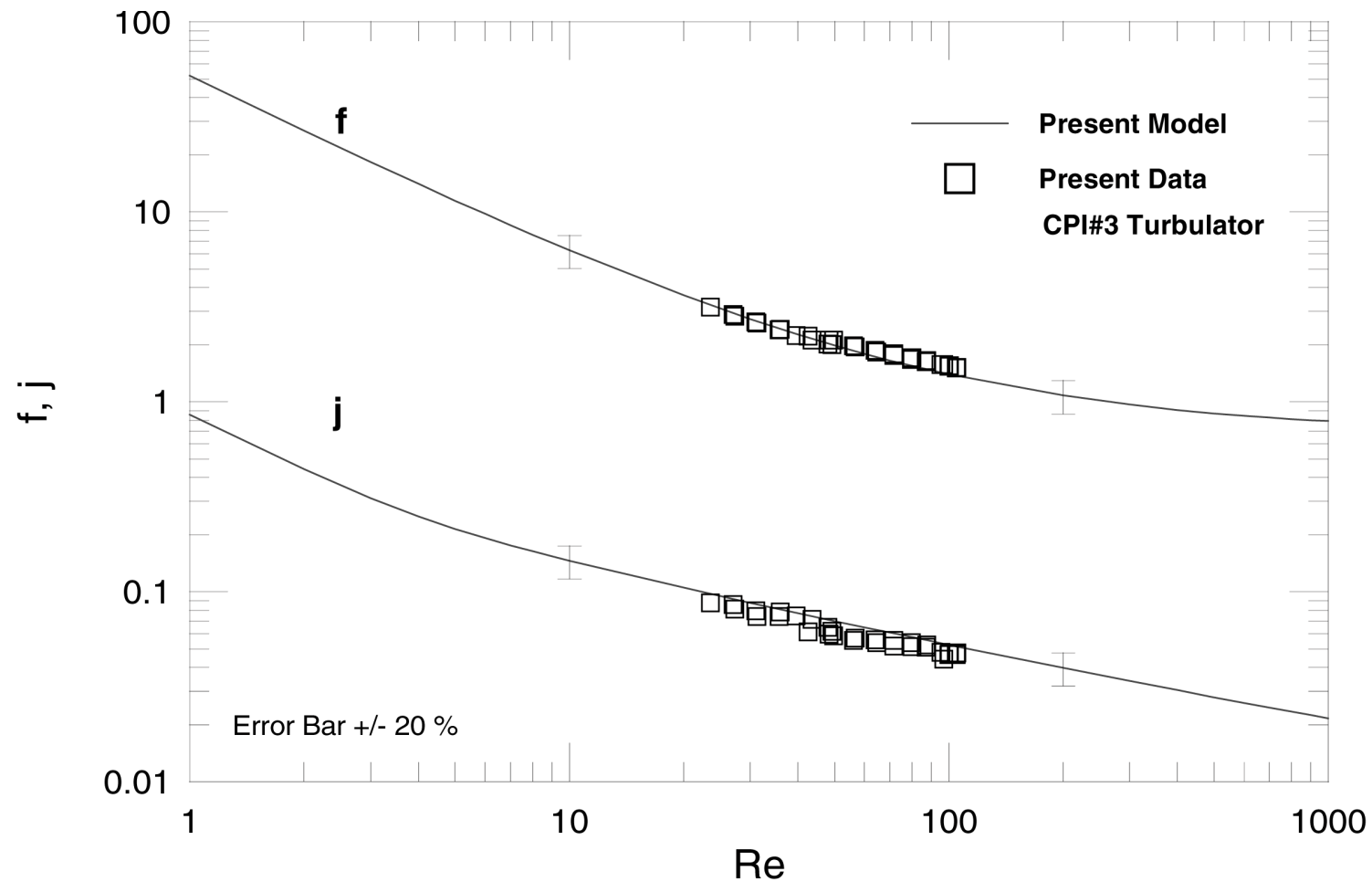
y_{cf} = low Reynolds number model (creeping flow)

y_{lam} = laminar flow model

y_{tur} = turbulent flow model

m, n = combination parameters Y. S. Muzychka and M. M. Yovanovich, HTD-
Vol. 364-1, 1999, pp. 79-90.

Model Validation



References

Lee, S., Lemczyk and Yovanovich, M.M., ``Analysis of Thermal Vias in High Density Interconnect Technology,’’ *Eighth IEEE SEMI-THERM Symposium*, pp. 55-61.

Hussien, M.M., Nelson, D.J. and Elshabini-Riad, ``Thermal Interaction of Semiconductor Devices on Copper-Clad Ceramic Substrates,’’ *Seventh IEEE SEMI-THERM Symposium*, pp. 117-122.

Elenbaas, W., ``The Dissipation of Heat by Free Convection: The Inner Surface of Vertical Tubes of Different Shapes of Cross-Section’’, *Physica IX*, No. 9, September 1942, pp. 865-874.

Churchill, S.W., ``A Comprehensive Correlating Equation for Buoyancy-Induced Flow in Channels,’’ *Letters Heat Mass Transfer*, Vol. 4, 1977, pp. 193-199.

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Raithby, G.D. and Hollands, K.G.T., "A General Method of Obtaining Approximate Solutions to Laminar and Turbulent Free Convection Problems," *Advances in Heat Transfer*, Vol. 11, edited by T.F. Irvine and J.P. Hartnett, Academic Press, New York, 1975, pp.

Muzychka, Y.S. and Yovanovich, M.M., "Modeling the f and j Characteristics for Transverse Flow Through an Offset Strip Fin at Low Reynolds Number," *HTD-Vol. 364-1, Proceedings of the ASME, Heat Transfer Division-1999*, Volume 1, ASME 1999, pp. 79-90.